A Low Power High Speed Mobile Memory I/O Interface Using Reconfigurable Multi-Band Multi-Modulation Signaling

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A LOW POWER HIGH SPEED MOBILE MEMORY I/O INTERFACE USING
RECONFIGURABLE MULTI-BAND MULTI-MODULATION SIGNALING

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A LOW POWER HIGH SPEED MOBILE MEMORY I/O INTERFACE USING RECONFIGURABLE MULTI-BAND MULTI-MODULATION SIGNALING

A Dissertation Presented to the Graduate Faculty of
Bobby B. Lyle School of Engineering
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in
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Doctor of Philosophy with a
Major in Electrical Engineering
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A Low Power High Speed Mobile Memory I/O Interface using  
Reconfigurable Multi-band Multi-modulation Signaling

Advisor: Professor Duncan MacFarlane

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This research mainly focuses on the design of a novel memory I/O interface with high bandwidth and high energy-efficient for mobile computing systems in order to dramatically enhance the circuit and system bandwidth and power efficiency. The proposed memory I/O interface, exploiting multi-modulation and multi-band signaling, is capable of supporting simultaneous bidirectional data transition of 4 separate data streams across a single-ended off-chip transmission line to achieve both high speed data rate and low power consumption. This multi-band multi-modulation interface (MMI) consists of multiple RF-band transceivers which utilize ASK modulation, and baseband transceivers which utilize 4-PAM modulation to increase the I/O bandwidth while supporting simultaneous bidirectional communication. The MMI circuit was implemented in 65nm CMOS process technology. Testing results show that the MMI interface achieves an overall data rate of 14Gb/s/pin and a better energy efficiency of 2.8pJ/b/pin compared to prior works.
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LIST OF ABBREVIATIONS

I/O  Input Output
CPU  Central Processing Unit
GPU  Graphic Processing Unit
DRAM Dynamic Random-Access Memory
RF   Radio Frequency
MMI  Multi-band Multi-modulation Interface
ASK  Amplitude Shift Keying
OOK  On-Off Keying
PAM  Pulse Amplitude Modulation
PLL  Phase-Locked Loop
DLL  Delay-Locked Loop
DDR  Double Data Rate
GIO  Global I/O
VCO  Voltage Controlled Oscillator
LO   Local Oscillator
C/A  command/address
RFTX RF-band Transmitter
RFRX RF-band Receiver
PAMTX PAM Transmitter
PAMRX PAM Receiver
DVFS Dynamic Voltage/Frequency Scaling
BALUN  Balance-Unbalance
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Chapter 1

INTRODUCTION

1.1. Introduction to Memory I/O Interface

About 2.6 billion mobile devices have been produced through 2016 in the application of communication and computing. In addition to this dramatic volume of production, more media-intensive functions such as enhanced graphic/image and media processing capabilities have been added to the mobile devices due to the convergence of communication and computing. However, mobile device power is already limited by the battery technology [1]. Therefore in order to support increasingly high performance under limited power supply, high-speed low-power circuitry became a popular approach.

Processors and memories are the major electronic components in mobile devices. As the development of semiconductor technology, memory bandwidth and processor speed has increased significantly. Main memories have developed from DDR1, DDR2 to DDR4 to support high speed and low power applications as shown in Fig. 1.1.

![Fig.1.1 Trend of DRAM performances [3]](image-url)
As shown in Fig.1.1, the performance of DRAM has been improved rapidly: the supply voltage decrease from 2.5V to 1.2V and the data rate increase from 0.2Gb/s/pin to 3.2Gb/s/pin [2]. Memory I/O provides communication between processor and memory. High bandwidth, high power efficiency and low latency memory I/O are needed to meet the development of processor and memory. Increasing the per-channel data rate and the I/O number are the two traditional approaches to increase memory I/O bandwidth [3]. The parallel memory I/O has multiple I/O interconnects transferring data simultaneously as shown in Fig.1.2. High data rate can be achieved. As interconnect number increases however, the signal suffers from crosstalk and power consumption increases. Also, total I/O number is limited by the chip packaging. Thus serial memory I/O with high bandwidth and low power consumption demands more attention.

![Parallel interface example](a) ![Serial interface example (MSB first)](b)

*Fig.1.2 Parallel interface and serial interface [4]*

Fig.1.3 shows the architecture of a typical serial memory I/O system. This memory I/O system consists of three major circuit components: the transmitter, the receiver and the timing system.
Fig. 1.3 Typical memory I/O system

The transmitter generates a required voltage swing and transmits it through the channel. Termination resistors are used to maintain impedance matching. Differential signaling is commonly utilized for common-mode noise rejection [3]. However, the capacitive and inductive coupling exist between the differential signaling lines which places I/O number limitation. This issue makes single-ended signaling popular in memory I/O system. The receiver recovers and amplifies the signal to a proper value. In the timing system, phase-locked loops (PLL) are commonly used to generate clock signal to synchronize the data. Forwarded-clock system is employed in this system and a dedicated channel is used to forward the clock signal.

PCB traces are typically used as the channel in memory I/O system. Fig.1.4 shows a demonstration of the memory I/O system with PCB trace. Wire-bonding is commonly used to connect the chip and the PCB trace. The PCB traces for memory I/O system are usually 5 to 30cm. The signal suffers from attenuation by channel impedance discontinuity, wire skin effect and dielectric loss of the PCB trace [3]. The loss of PCB trace channel becomes an important limiting factor of the memory I/O bandwidth.
Another issue in the memory I/O is the latency between processor and the memory. High speed data processing requires low latency. Short channel will help in reducing latency.

![PCB Diagram](PCB.png)

**Fig.1.4 Memory I/O system with PCB traces**

### 1.2. High Speed Interface in Mobile Memory

Multimedia related features such as high-quality gaming and video functionalities have been added to mobile devices due to the high integration of communication and computation [5]. Therefore the demand for high-speed, low-power, high-density mobile device has placed more restriction on the design of modern mobile devices. Due to the size and power limitation in a mobile device, its central processing unit (CPU), graphic processing unit (GPU) and memory subsystems are required to increase both bandwidth and energy efficiency constantly as mobile devices.

As mentioned above, the conventional memory interfaces may achieve the target data rate by using parallel I/O interconnect. However, these memory interfaces suffer from the signal integrity problems such as crosstalk between data and clock and large power consumption due to the increased number of parallel I/O interfaces. The total power consumption is effectively increased when increasing the target data rate of each I/O interface. Also, the latency between microprocessor and memory will be increased by increasing the required data sampling clock frequency. Therefore serial I/O interface is more preferred in nowadays applications.
One critical problem of modern memory I/O interface is that, it cannot satisfy the requirement of both high speed performance and low power consumption at the same time. Although Intel is developing the next generation memory interface base on multi-band structure, 80% of DDR memories are still implemented by point-to-point baseband-only structure as shown in Fig.1.5. Each channel (transceiver) only operates in one direction while carrying only one set of data stream. Therefore if the memory capacity is to be increased, the number of Global I/O transmission line (GIO) must be increased as well. In addition, as each of the channels is unidirectional, same numbers of channel is needed for return signal, which furthermore increased the number of GIO.

![Memory interface configuration of modern DDR memory](image)

*Fig.1.5 Memory interface configuration of modern DDR memory [6]*

As a result, the total power consumption and the total area of the interface will be increase dramatically due to the increased number of parallel I/O transmission lines, which makes these memory interfaces suffer from unavoidable signal integrity problems such as crosstalk between data and clock. Another problem that increases the power consumption of the current memory I/O interface is that they are not reconfigurable. Like in DRAM, it supports a fixed channel configuration between memory controller units.
(MCU) and shared DRAMs. Meaning that even there are only a portion of channels processing data, all channel need to be turned on to support the operation. Therefore it seriously increases unnecessary power consumption during operation.

1.3 Related Works of Improvement

Five years after the first DDR memory, a creative RF/baseband FDMA interface [7] was invented in 2005 as indicated in Fig.1.6. Except using the conventional baseband only transceiver, it introduced an extra RF-band transceiver, which utilized BPSK modulation. Both RF-band and baseband share a single transmission line. In such an idea, simultaneous bidirectional and reconfigurable data communication is realized, while reducing the number of GIO into half.

![Block diagram of RF/baseband FDMA interconnect](image)

Fig.1.6 Block diagram of RF/baseband FDMA interconnect [7]

However, BPSK modulation demands strictly on both phase and frequency synchronization between the transmitter and receiver [8]. Thus, a frequency synchronization circuitry like a PLL, which is power hungry and complicated in design, is needed for each RF-band transceiver. In addition, since RF and baseband signals are directly coupled, a power hungry and area costing narrow-band filter is needed in each RF-band receiver to filter out the unwanted signal for data recovery. Therefore even this interface can reduce the number of GIO into half of the original value, the cost of power consumption and chip area is still very high.
Another successful attempt was made in 2011, called Dual-Band Bidirectional Interface [9], as indicated in Fig.1.7. Its basic idea is pretty much same as [7], which combines RF-band and baseband transceivers while sharing single transmission line. In this design, the RF-band transceiver utilizes ASK modulation which the carrier frequency is provided by a free VCO. This in turn loosened the requirement of LO signal phase and frequency accuracy compared to [7], therefore eliminated the complicated power hungry PLL in the design. In addition, the coupling transformers implemented at both sides of transmitter and receiver enable direct signal coupling/splitting without bandpass filter. Therefore this design successfully achieved simultaneous bidirectional data communication of two data streams over a single transmission line without consuming a lot of power and area.

![Fig.1.7 Block diagram of dual-band bidirectional interconnect [9]](image)

However, since this design only allows two signal bands sharing the transmission line, and multiplies the data rate by 2, it still does not satisfy the data rate growth in modern memory after many years. Therefore researchers are triggered to seek better ideas to add more bands of transceivers.

Just three months before this dissertation was written, a promising tri-band serial link was published [10]. Although it was not a complete I/O interface since they only
designed the transmitter of the link without including the receiver, this new idea incorporates one baseband transmitter, and two RF-band transmitters with carrier frequency of $f_1$ and $f_2$, respectively. The baseband and RF-band signals are summed together implementing a tri-band transmitter which supports an overall transmitting data rate of 16Gb/s through a differential channel, as indicated in Fig.1.8.

![Tri-band Cognitive Serial Link Transmitter Diagram](image)

**Fig.1.8 Block diagram of tri-band cognitive serial link transmitter [10]**

The tri-band transmitter in [10] combines two 64-QAM RF-band transmitters and an 8-PAM baseband transmitter, therefore it will be very challenging to design an on-chip receiver for this kind of complicated transmitter, therefore in [10] it used instrumental receiver. For instrumental testing, the transmitter in [10] requires a differential channel (i.e., cable), resulting in reduced-by-two per-pin data rate.
1.4 Research Objective

In order to solve the aforementioned problem, a new idea for memory interface is proposed as shown in Fig.1.9.

![Block diagram for demonstration of proposed new idea](image)

*Fig.1.9 Block diagram for demonstration of proposed new idea*

The basic idea is to improve the data rate between memory banks and reduce the number of GIO channel to reduce power consumption and chip area at the same time. Also the reduction of the numbers of GIO channels must still maintain simultaneous data transmitting/receiving. Here we introduce a new kind of memory interface, indicated by the blue blocks. This kind of interface transmits four data streams simultaneously and bidirectionally. Through a variety of signal modulations, four data streams are combined into a single stream of mixed signal. This single mixed signal stream will then be sent to the destination memory bank, from which it will be demodulated and recovered into the original 4 four data streams for further processing. Therefore, the numbers of GIO channels are reduced to ¼ of the original value. It also increases the value of overall data rate four times higher than the original value. The chip area and power consumption is
greatly decreased due to the reduced number of GIO. Furthermore, as of data reconfigurable capability, this interface allows controllable power supplies among all four data streams through power management unit. In that case if there is no data input to a channel, the channel will be automatically shutdown to save power consumption.

**Fig.1.10 System configuration of the Proposed MMI**

The proposed new I/O interface is called multi-band multi-modulation interface (MMI), as demonstrated in Fig.1.10. Unlike the conventional point to point, baseband only signaling used in DDR memory, the proposed MMI interface utilizes multi-band and multi-modulation signaling to achieve an overall data rate four times higher than the conventional structure. The MMI system consists of two RF-bands which utilize ASK modulation and Baseband which utilizes a 4-level pulse-amplitude modulation (4-PAM). Data streams $D_1$ and $D_4$ are modulated by ASK modulation through the RF-bands, and
data streams $D_2$ and $D_3$ is modulated by 4-PAM modulation through baseband. Therefore two sets of ASK signal and one set of 4-PAM signal is created through multi-modulation.

As shown in Fig.1.10, a novel band-select transformer is placed at both sides of the transceiver. This band-select transformer can be considered as connecting the secondary coil of two regular transformers together to make a three port transformer. Therefore it consists of two primary coils in different size and one secondary coil. Although it is simple to observe its physical shape, the design and analysis of this band-select transformer is relatively complicated. Two ASK signals are sent to each primary coil of the transformer and coupled together to the secondary coil. The low frequency PAM signal is sent to the secondary coil directly. Therefore the modulated ASK and PAM signals are coupled by the band-select transformer into an intermediate mixed signal which consists of both RF and baseband frequencies. This novel band-select transformer has not been designed before for memory interface.

The intermediate mixed signal from the band-select transformer is then transmitted through the single ended off-chip transmission line into the MMI receiver. Signal splitting at the receiver side is also performed by the band-select transformer at the receiver side. Once the secondary coil of each regular transformer at the receiver side senses the intermediate mixed signal, it filters out the unwanted RF-band frequency and provides the remaining in-band ASK data into the RF receiver. For baseband signal, it simply travels through the metal wire of the secondary coil of both the transformers and the transmission line, to the baseband receiver. Therefore, after the ASK and PAM signals are demodulated by their receivers, the original four input data are then recovered at the output.
Therefore this MMI system can simultaneously transmits/receives four data streams in both directions on a single-ended off-chip transmission line between the Memory Control Unit (MCU) and the Memory. By applying the MMI interface to LP-DDR I/O data (DQs) and to the command/address (C/A), the mobile DRAM access time can be significantly reduced by requesting simultaneous read/write-operations on a shared memory interface.

Clock distribution circuitry is also shown in Fig.1.10. Due to the long distance routing of clock signal, the clock phase of transmitter and receiver needs to be synchronized. This is implemented by a delay-locked loop (DLL) as indicated in Fig.1.10. DLL is a popular clock generator in any DRAM design. In a modern memory design, one of the important hurdles is that the valid data window varies according to the PVT variations. For example, in a DDR memory, it is harder to obtain a valid data window than the SDR one. The MCU cannot have a valid sampling position. Therefore, in order to transfer data with higher speed, the timing variation according to PVT variations should be reduced by using DLL.

The main objective of this research is focused on developing a revolutionary memory interface which utilizes multi-band and multi-modulation signaling to achieve quadrupled (4x) data rate and improve the energy efficiency for future mobile devices compared to traditional design. This Multi-band Multi-modulation I/O Interface (MMI), unlike the conventional base band only signaling consists of two RF bands, both of which utilize ASK modulation and a baseband which utilizes 4-level pulse-amplitude modulation (4-PAM). In this case that it can simultaneously transmits or receives four data streams in both directions on a single-ended off-chip transmission line between the
Memory Control Unit (MCU) and the Memory. Therefore the MMI bandwidth achieves four times that of the conventional memory interface. Three specific tasks will be carried out in detail to fulfill this objective:

Task1: Design two RF-band transceiver with carrier frequencies separated widely enough for signal filtering.

Task2: Design an energy efficient 4-level pulse-amplitude modulation transceiver for the baseband channel.

Task3: Design a 3 port band-select transformer which serves as a filter for RF band transmitting/receiving.
CHAPTER 2
RF BAND TRANSCEIVER

2.1 Introduction

The RF-band transmitter (RFTX) uses an ASK modulator to modulate the incoming data before sending to the single-ended transmission line. The clock frequency of the transmitter is generated by VCOs. The receiver side employs a differential self-mixer to demodulate the ASK signal. After that, the differential amplifiers boost the demodulated signal for further data recovery. Testing results show the RF transceiver operates at a data rate of 3Gb/s/pin while consumes 12mW power.

The ASK modulators in each RF-band transmitter has different carrier frequencies which are provided by free voltage-controlled oscillator (VCO), each operates at 12.3GHz and 24.6GHz respectively for signal modulation. Due to the nature of ASK modulation, the requirement of phase noise of VCO output signal is low, therefore a free VCO is sufficient in the design, although its output frequencies are relatively noisy. Input data of each RFTX is applied on the transmission gates of ASK modulator. By controlling the ON/OFF status of the incoming RF frequencies, the ASK modulator converts the input data ASK signal with RF frequency. The ASK signals are further amplified through output driver before sending to the primary coils of the band-select transformer.

For the RF receiver design, a differential mutual (self) mixer is implemented as an envelope detector to down-convert the ASK signal to baseband signal by tracking the
envelope of the ASK signal. The envelope of the ASK signal is essentially the original input data. Therefore, the self-mixer that is capable of performing direct-down conversion of ASK signal to the original baseband input signal. The mutual mixer is followed by a buffer converter with resistive feedback. This buffer converter automatically stabilizes its input and output common-mode voltage and amplifies the recovered baseband signal to a full-swing rail-to-rail digital signal for the final output.

2.2 Design of RF-Band Transmitter

The RF transmitter architecture consists of the three blocks: low-noise voltage controlled oscillator (LNVCO), input buffer and ASK modulator as demonstrated in Fig.2.1. Although ASK modulation places less requirement on the phase noise of the carrier frequencies, as described in previous session, it is still necessary to keep the phase noise relatively low, because of sharp filtering of the band-select transformer for signal splitting at receiver side. Therefore a low-noise voltage controlled oscillator is designed to provide the carrier frequencies with a phase noise as low as -114dBc/Hz at 1MHz offset from fundamental output frequency.

Fig.2.1 Schematic of ASK modulator in MMI
Fig. 2.2 shows the schematic of the conventional VCO with tail current source. The white noise of the tank (L₁ and C₁) which provides output oscillation and the differential pair which provides negative resistance are intrinsic noise sources. They cannot be removed or suppressed. However, the flicker noise from the differential pair and tail current source as well as the white noise of the tail current source may be effectively reduced by some techniques. These techniques include: (i) removal of tail current source, (ii) LC noise filtering, (iii) hybrid capacitance.

![Schematic of conventional VCO with tail current source](image)

*Fig. 2.2 Schematic of conventional VCO with tail current source*

As pointed out by the phase noise model [11], the tail current source contributes more phase noise when the oscillation amplitude is large. Therefore, removing the tail current source is helpful to get rid of the phase noise from the tail current source [12][13][14]. However, one problem needs to be taken care of before simply removing the tail current source. The removal of tail current source also reduces the impedance at the common-mode point S, which actually reduces the resonator quality factor because of
the load effect [15]. At zero differential oscillation voltage, two coupled transistors evenly share the tail current and both of them are in saturation. As the rising of differential oscillation voltage crosses $V_{th}$, the $V_{gd}$ of one MOSFET exceeds $V_{th}$, forcing it into the triode mode, and the $V_{gd}$ of the other MOSFET falls below $-V_{th}$, driving it deeper into saturation. The on resistance $r_{ds}$ of the device in the triode region decreases with the differential voltage and adds greater loss to the resonator because the current flowing through it is in-phase with the differential voltage. In the next half cycle, the same situation occurs to the other MOSFET. Hence, as the load of the resonator, the two transistors lower the average resonator quality factor. With a smaller resonator $Q$ factor, the phase noise of the oscillator increases [36]. On the other hand, if a current source with relatively large output impedance is inserted into node S, the load impedance “seeing” by the sources of the MOSFETs is always high, resulting in negligible current through $r_{ds}$. Hence, it preserves the $Q$ factor of the resonator. Due to this drawback, if the tail current source of the LC oscillator is to be removed, another method needs to be applied in order to maintain a significant phase noise improvement.
Fig.2.3 Schematic of LNVCO with phase noise reducing techniques

Other than providing the constant bias current, the tail current source also places high impedance in series with the switching MOSFETs of the differential pair. As discussed above, reducing the impedance degrades the $Q$ factor of the resonator and thus increases the phase noise. On the other hand, it is well known that the common mode node of the differential pair is a “virtual-ground” point (low impedance point) for the differential signal. In any balanced circuit, odd harmonics circulate in a differential path, while even harmonics flow in a common-mode path, through the resonator capacitance and the switching MOSFETs to ground in this case. Therefore, strictly speaking, it is only necessary to provide high impedance to even harmonics at the common-mode point. If the noise near the second-order harmonics is dominant, it suggests that a high impedance, narrow band circuit centered at $2\omega_0$ can be added to the common mode point of the LC oscillator as indicated in the red box of Fig.2.3. In this oscillator, the inductance $L_2$ is chosen to resonate at $2\omega_0$ in parallel with the overall capacitance
presented at the node \( S \), i.e. \( C_2 \). Hence, the impedance for second-order harmonics is raised, and the \( Q \) factor is preserved. The high impedance \( LC \) filter circuit also blocks the noise from ground near the frequency of \( 2\omega_0 \).

Another technique involved to reduce phase noise is called hybrid capacitance as indicated in the blue box of Fig.2.3. According to separated phase noise simulation of each device in the VCO, variable capacitor contributes the most noise, even higher than the cross coupled capacitors. Therefore reducing the noise from the variable capacitor will greatly reduce the overall phase noise of the VCO. Although we can use fixed-value noise-free capacitors, the consequence for doing that will be risky. As the value of the capacitor is fixed, so is the output frequency of the VCO. Even we can mandatorily set the output frequency to the resonant frequency of the band-select transformer for filtering, the value may drift due to PVT, therefore a small range of frequency variation is still necessary. The tuning range will be unnecessarily wide if the capacitance of the resonant LC tank is provided by the variable capacitor, so in this design, only a small portion of the variable capacitance is available, leaving the majority of capacitance provided by the fix value capacitor. In such a case, the overall noise from variable capacitor is greatly reduced. In other words, we traded off the unnecessary frequency tuning range with noise performance. Fig.2.4 shows the transient simulation result of the VCO output, which provides carrier frequency for the ASK modulator.
Fig. 2.4 Transient simulation result of LNVCO output frequency

Fig. 2.5 Phase noise simulation of LNVCO

Fig. 2.5 shows the simulation results of phase noise at all frequencies, the phase noise at 1 MHz offset is -114 dBc/Hz, which is a very low value ever achievable by a free VCO. Therefore even the switches in ASK modulator add in some extra noise, the overall phase noise appears at the RF-band receiver is still reasonably low for recovery.
The LNVCO’s output is the carrier signal that will be modulated by the input data as indicated in Fig.2.1. The ASK modulator accepts input from the LNVCO and the input buffer. In this case, it allows the carrier frequency to feed-through only when the input buffer signal is high. This is the final output that is sent to the transmission line. This type of modulation is sometimes referred to as on-off shift keying (OOK).

Fig.2.6 ASK modulator switch for RF-band transmitter

One critical aspect of implementing ASK modulation in CMOS process is the design of good high-speed switches. Since we can visualize ASK modulation as a carrier signal (output frequency from the LNVCO) being able to pass to the output if the switch is turned on when data is at logic high, but should not be able to if the data is at logic low. Figure 4.2 shows the Ask modulation configuration. The data stream outputted by the input buffer modulates the carrier by switching on/off the current flow through transmission gates M3-M4 and M5-M6 to complete the ASK modulation. A transmission gate M7-M8 is also employed in the ASK modulator to make a fast shut off at the output.
Using this switch reduces the amplitude of non-modulated signals. The inductor used in the ASK modulator has a center tap which is connected to the power supply to be given to the modulator.

Fig.2.7 Schematic of RF-Band Transmitter

Fig.2.7 shows the schematic of RF-band transceiver. The 12.3GHz and 24.6GHz carrier frequencies are generated by the LNVCO in each individual ASK modulator. The differential ASK output signal is coupled to the off-chip transmission line via the on-chip band-selective transformer which the design process will be discussed in the later chapter. Due to this on-chip transformer’s inherent impedance transformation, the impedance matching complexity is significantly relaxed. By sizing and determining the turn-ratio of an on-chip transformer, the reflected wave from the off-chip transmission line can be reduced greatly.

In order to minimize the dispersion of the RF carrier signal, the RF carrier to target data rate ratio is also extremely critical by considering the reasonable signal loss of the off-chip transmission at the same time. By this careful consideration of impedance
matching and reduced dispersion of RF carrier, the power hungry pre-emphasis circuit at transmitter and complicated equalization at receiver can be removed, resulting in reduced chip area and power consumption of transceiver. Fig.2.8 shows the simulated input and modulated output signal of the ASK modulator in 65nm CMOS process technology. The input data stream at the top is 5Gb/s of random data generated by PRBS generator. The Output data at the bottom exhibits the ASK-modulated random data output stream after startup time.

2.3 Design of RF-Band Receiver

The RF transmitter architecture consists of the three blocks: self-mixer, buffer converter and output driver together with several stages of baseband amplifiers as demonstrated in Fig.2.9. According to the signal waveforms of each stage, it is intuitive to grasp the basic idea of how the RFRX works.
In the RF receiver, the differential active self-mixer is the key block as demonstrated in Fig.2.9. It amplifies the incoming ASK modulated RF carrier, which is attenuated by the loss of off chip transmission line. Then as an envelope detector the self-mixer down-converts the RF carrier into the original baseband signals. In other words, the RF receiver design features a mixer that is capable of non-coherent direct-down conversion to a baseband signal from the carrier frequency. Comparing this fully differential active mixer to the conventional single-ended or passive mixers, the later ones suffer from either substantial signal loss at high frequencies or being very sensitive to supply noise coupling.

The self-mixer is followed by a buffer converter with RC feedback. Input common-mode voltage of the buffer converter could be set down by itself when amplifying the recovered baseband signal. Then the signal is recovered to a full-swing rail-to-rail digital signal. The mixer operates under the design principles of the well-known Gilbert-cell Multiplier circuit [39][40][41][42], where ASK signal from RF-band transmitter is applied to both RF and LO inputs of the mixer (self-mixer). Therefore the ASK signal is down converted to baseband signal which is the original data.
The active self-mixer amplifies and down-converts the modulated RF carriers by feeding ASK modulated signals to differential gates and drains, which are the inputs of a regular Gilbert-cell mixer. This active self-mixing scheme with subsequent differential amplifier will generate differential outputs to the baseband output driver. Because the receiver of ASK demodulation scheme only senses the amplitude change of a RF carrier signal, there is no need to detect and synchronize frequency or phase variation, which resulting in much simple receiver architecture.

The idea of self-mixer comes from multiplication of the two sinusoidal input signals. These two signals can be expressed as:

\[
S_1 = A \cos(\omega_1 t + \varphi_1)
\]

\[
S_1 = A \cos(\omega_1 t + \varphi_1)
\]

By applying product-to-sum trigonometric identity and then rearranging factors, we can get two frequency tones from the self-mixer output:

\[
S_1 \times S_2 = -\frac{AB}{2} \left[ \cos((\omega_1 + \omega_2)t + (\varphi_1 + \varphi_2)) - \cos((\omega_1 - \omega_2)t + (\varphi_1 - \varphi_2)) \right]
\]

(3.3)

The first signal is in additive form and the other in subtractive form. The first term is the high frequency image signal, which could be filtered out. The second term is baseband signal. Therefore, if two identical signals are applied, they could be theoretically converted directly down to baseband. The additive signal will be filtered out in subsequent circuit blocks, while the binary baseband data will be amplified rail-to-rail for transmission line.
Fig. 2.10 shows the conversion gain of the self-mixer under different input power level. It shows that when the input power level is between -10dBm to -2dBm, the self-mixer achieves a conversion gain close to its maximum value of 10dB, therefore the input power of the self-mixer need to be adjusted to between 10dBm (200mV<sub>pp</sub>) to -2dBm (500mV<sub>pp</sub>). Fig.2.11 also shows the output spectrum of the self-mixer. It clearly indicates that odd order harmonic has greatly been suppressed leaving only even order harmonics including DC envelope signal. This means the self-mixer has high conversion gain, and high isolation between input and output.

Simulated input and output signals of the differential self-mixer are shown in Fig.2.10. The amplitude of the received signal is reduced to 400mV due to the loss of transmission line. This power level is more than sufficient as the mixer input. Also this value is carefully calculated to meet the input power range for maximum conversion gain of the self-mixer.
From the output waveform of Fig.2.10, it is obvious that the upper peak value of the signal at one output node is the lower peak value of the other, this is due to the method of envelope tracking of the self-mixer. This means the differential output signals are based on two different common-modes, which may cause a problem for subsequent baseband differential amplifiers since the input voltages are not balanced. Therefore, the
buffer converter with RC-feedback is introduced to equalize common-mode voltage of the mixer output signal for the succeeding baseband amplifiers.

![Fig.2.11 Schematic of buffer converter with RC-feedback](image)

Fig.2.11 shows the schematic of the buffer converter. The RC feedback circuitry acts as low pass filter to further filter out high frequency components from mixer output. Since the settling time depends on the RC feedback network, a very large resistance of 400kΩ with a capacitor of 128fF was chosen for the best transient response. According to the output waveform of the buffer converter in Fig.2.12, the output common-mode voltage is equalized.

![Fig.2.12 Input and output waveform of buffer converter](image)
The components following the buffer converter include baseband amplifiers and output driver. Fig.2.13 shows the circuit configuration of the three-stage differential amplifiers used in the system. All three differential amplifiers have different load resistor and biasing current values. The values of the load resistors are in high to low order while the values of biasing current are in low to high order. In such a case, the amplifier chain can drive very large input load of the output driver. In addition, the differential amplifier also helps to amplify the signal and removes the higher order harmonics present in the signal as shown in Figure 2.10.

![Schematic of the cascaded baseband amplifier](image)

**Fig.2.13 Schematic of the cascaded baseband amplifier**

Since there are two RF-band transmitters in the MMI system for two data input, there are two RF-band receivers for individual data recovery. Fig.2.14 shows the connection of whole RF-band receiver with the on-chip band-select transformer. The transmitters and receivers exchange data through a 5cm off-chip transmission line which is mounted on a FR-4 PCB board.
Fig. 2.14 Complete schematic of RF-band receiver

Fig. 2.15 shows the simulated waveforms of single RF-band ASK transceiver of the MMI system, which fully recovers the original input data stream by ASK (de)modulation technique without any frequency and phase synchronization. Furthermore the ASK RF-Interconnect does not suffer from process-induced RF-carrier variation between the transmitter and receiver. The RF-Interconnect can be also compatible to a CMOS technology and it can operate fully with traditional digital logic circuits placed directly under its on-chip passives such as an on-chip transformer and inductors, which results in much reduced layout area. In conclusion, without the needs of power-hungry frequency and phase synchronization, a simple RF-band transceiver architecture provides potential advantages that ASK RF-interconnect can be power-efficient and applied to
future advanced memory interface of challenging situation of chip-to-chip communication.

Fig. 2.15 Recovered RF-band output waveform of the output driver (upper: self-mixer input, lower: recovered data)

2.4 RF-Band Transceiver

Fig. 2.16 shows the complete RF-band transceiver architecture where both channels use ASK modulation scheme. The system consists of a two ASK modulators under different carrier frequencies, an off-chip transmission line with two on-chip band-selective transformers, and ASK demodulators.
Fig. 2.16 Complete schematic of RF-band transceivers

Fig. 2.17 shows the eye-diagrams of the output data of the two RF-band transceivers. The opening-eyes indicate fully recovery of the original input data stream.
which is implemented by ASK (de)modulation technique without any frequency and phase synchronization. In addition, since the RF-band transceivers do not suffer from process-induced RF-carrier variation between the transmitter and receiver, the RF-band transceiver can be also compatible operate properly with CMOS logic circuits placed directly under its on-chip band-select transformers, which results in much reduced layout area. This will be covered in later chapters. In conclusion, without the needs of power-hungry frequency and phase synchronization, a simple RF-band transceiver architecture provides potential advantages that ASK based RF-band transceiver can operate at high speed and be power-efficient, and could be applied to future advanced memory interface under challenging situations of chip-to-chip communication.

Fig.2.12 Eye diagram of the output data of RF-band receiver
CHAPTER 3

FOUR-LEVEL PULSE AMPLITUDE MODULATION (4-PAM) TRANSCIEVER

3.1. Introduction

The other half portion of the MMI I/O interface for Mobile DRAMs is presented based on four-level pulse amplitude modulation (4-PAM). Other than the two RF-band transceivers from previous chapter, two more data streams were carried by pulse 4-PAM transceiver in the baseband channel of MMI. The PAM transceiver uses a current mode transmitter and a dual-sampling receiver to transmit and receive two data streams through a shared single ended channel simultaneously. The transmitter employs a voltage mode output driver which sends modulated 4-PAM data through the channel. The receiver side uses differential amplifier based comparator to decode three voltage levels by comparing the PAM signal with three reference voltages. The transceiver is simulated in 65nm CMOS technology at 1.2V. The results show the increase of the data bandwidth to 8Gb/s. Energy efficiency of mobile PAM I/O memory interface is 2.1pJ/bit.

3.2. 4-PAM in Modern I/O

In order to increase channel bandwidth, serial link has become popular due to its high speed and low power consumption [25] for mobile memory I/O interface. However, long initialization time of serial links does not meet the requirement for high switching I/O [26][27][46]. Therefore a four-level pulse amplitude modulation (4-PAM) transceiver becomes a more preferable choice since an N-PAM signaling technique can reduce the
symbol rate by a factor of \( \log_2 N \) compared with baseband only signaling [28]. The proposed PAM transceiver utilizes a novel encoder/decoder and dual-sampling technique to transmit and receive two data streams through a shared single-ended transmission line simultaneously. Two types of PAM transceiver are available in modern application, current mode [29][30][31] and voltage-mode [32][33][47]. The proposed dual-sampling 4-PAM transceiver is implemented in voltage-mode due to its fast switching time. It supports two data stream communication simultaneously. The implementation of 4-PAM in MMI system is demonstrated in Fig.3.1. It is connected directly to the secondary coil of the band-select transformer.

Fig.3.1 Implementation of 4-PAM transceiver in MMI system
3.3. Design of PAM Transmitter

The PAM transmitter consists of a 4-bit encoder, a DFF, and a voltage mode driver as shown in Fig.3.2. Two data streams, $D_2$ and $D_3$, are encoded by the encoder, converting the dual data into 4-bit encoded control signals according to logic level combination among two data streams. A 4-bit synchronizer (DFF $[3:0]$) generates a synchronized encoded signal to reduce the latency skews of the encoded signals. The PAM transmitter uses a voltage mode output driver to generate a 4-level voltage output signal representing the 4 encoded bits. An impedance controller is used on both sides of the on-chip transformer and in the PAM transmitter output driver to set the common mode voltage at the transformer center tap and to remove the impedance mismatch.

![Fig.3.2 4-PAM Transmitter schematic](image)

The PAM transmitter generates 4-level bidirectional signaling. Transistor switches in a conventional PAM transmitter can create a leakage current in the transmission line due to leakage current created by multi-level driver. So we added a novel leakage suppression control logic block to reduce the leakage current in DRAM power-down/nap mode. The encoder outputs (cs0 to cs3) are connected to transistor switches. When the control logic circuit output (PAM_ENC) is 1 (logical high), the switches are turned off in DRAM power-down mode to save all leakage power. If the
state of PAM_ENC is changed to 0, the PAM transmitter perform normal operation in DRAM active (or active standby) mode. Thus, if the memory is in an active-standby mode for a long time, the proposed PAM transmitter doesn’t degrade the data read/write performance. Fig.3.3 shows the schematic of the encoder logic.

As the first stage of the PAM transmitter, several critical considerations need to be taken care of when designing the encoder. The most important one is how to reduce the bit error to the uttermost. Since 4-PAM hard decision decoding (comparator) is used in the receiver, the bit error is due to the comparison error between the multi-level PAM signal and the three DC reference levels of at the receiver side. Therefore a fixed one-to-one mapping of every two input bits to a constellation point must be chosen. Six distinct mapping exists for 4-PAM. However, only a Gray-code mapping guarantees that every nearest symbol error results in only one bit error. Thus, the expected bit error rate is reduced to that of the linear mapping. The advantage of Gray-code mapping is shown in Fig.3.4.
The encoder shown in Fig.3.3 converts the each dual data bits into a 4-bit encoded control signal en0, en1, en2, and en3 at each clock cycle. To reduce the latency skews of the encoded signal, a 4-bit synchronizer implemented by D flip-flops (DFF) is utilized to generate a synchronized encoded signal (cs0, cs1, cs2, and cs3). These four bits of synchronized codes are applied to the PAM driver to generate multi-level PAM signal. The schematic of the PAM driver is shown in Fig.3.5.

When four bits of control codes are applied to the gates of the PAM driver, it generates different levels of voltage at the output node according to the pattern of the

---

**Fig.3.4 Linear versus Gray code mapping of levels**

**Fig.3.5 Schematic of PAM driver**
control bits. The voltage sources are ground, half VDD (HVDD), and VDD. Therefore in this design, the output levels are ground, (HVDD + ground)/2, (HVDD + VDD)/2, and VDD.

The output of the PAM driver is connected directly to the secondary coil of the band-select transformer. It eventually drives the 5cm transmission line. Therefore, a digital impedance control logic circuit is used to control the output impedance of the PAM driver to achieve maximum power delivery onto the transmission line. The impedance control circuit is composed of multiple binary-weighted switches and resistors to provide digitally controllable driver strength by selectively enabling the resistors. Regardless of the process–voltage–temperature variations, there are sufficient control codes to control the driver strength, with the value of 100 ± 15 Ω matching the required resistance to the impedance of the off-chip channel.

One issue was noticed after the design of the PAMTX is that the idea of using only three voltage sources to generate four output voltage levels might cause a slight variation (instability) of voltage level 2 and 3, therefore eventually affects the constellation of PAM signal. This is due to voltage “fighting” and ON resistance of MOS switches. The power supply with the higher voltage will discharge into the other one, until they end up with equal voltages. If the second battery (the lower voltage one) is a rechargeable, then it will be charged by the first one, again until the two have the same voltage. In this case the end voltage will be intermediate between the two starting voltages and their output resistances which are the ON resistances of each MOS switches. The current flowing between the batteries during this process will be quite high. It is equal to the different between the two voltages divided by the sum of the output
resistances of the power supply. Therefore a modified PAM driver will be proposed in future design as demonstrated in Fig.3.6. In this design, the voltage “fighting” will be eliminated by using one more DC voltage source. And of course the encoder logic also needs to be redesigned to turn on only one switch in the modified PAM driver at each clock cycle. This in turn stabilize the output DC voltage levels therefore improve the quality of PAM constellation. However the draw back for this structure is that we need to add in one more precious I/O pad for the chip.

![Impedance Controller](image_url)

*Fig.3.6 Modified schematic of PAM driver*

Another issue comes from direct coupling of PAM driver with the secondary coil of the band-select transformer. The two transformers are terminated by 50Ω resistors as shown in Fig.3.7. The resistors are connected to power supply V\textsubscript{dd} and ground, therefore setting the DC biasing voltage of the transmission line to V\textsubscript{dd}/2=600mV.
However, if the PAM driver is directly connected to the secondary coil of the transformer the impedance will be varied when output voltage level of the PAM driver shifts, as shown in simplified schematic in Fig. 3.8 where parasitic resistance of the transformer has been neglected. Therefore in this case, whenever the $V_{PAM}$ switches due to control code, it shifts the DC biasing of the transmission line away from 600mV. This variation eventually uneven step size of the multi-level PAM signal.

Fig.3.8 DC biasing variation on the transmission line

Fig.3.9 shows a clear 4 level PAM waveform at the output of PAM transmitter. This 4-PAM signal is sent to the off-chip transmission line to PAM receiver.
3.4. Design of PAM Receiver

PAM receiver consists of three comparators, voltage generators, a dual-sampling D flip flop (DS-DFF), a digital impedance controller, and the output driver. In order to recover the data from the incoming 4-PAM signal of the transmitter, the receiver should have low offset, high resolution and low latency characteristics in both voltage and time domains. The incoming 4-PAM data from the channel is sent to the comparators which effectively recover the data from the channel by using reference voltages selected sampling. The data is compared with the reference voltages and then the output comparison data from comparators is decoded to 4-bit binary data. Fig. 3.10 shows the schematic of the novel source-synchronous 4-PAM receiver with a dual-sampling bit-synchronized decoder and digitally controlled impedance logic.
The comparator is composed of a two-stage amplifier. The first-stage amplifier compares the incoming PAM signal with each reference voltage. The second-stage amplifier converts the first-stage output to rail-to-rail complementary signals for next-stage DFFs. The 4-PAM levels are at 280, 370, 450, and 580 mV, respectively, and the reference voltages (vref1, vref2, and vref3) of the comparators are at 310, 410, and 510 mV, respectively. Simulation results show that the input offset voltage of the comparator is 2.08 mV. Therefore, the gaps between the PAM levels and the reference voltages are enough for the comparators. The input sensitivity of the comparator is ±50 mV to amplify the incoming PAM signal reliably. Fig.3.11 shows the schematic of the comparator.

Before PAM decoding, the proposed dual-sampling DFF (DS-DFF) is added between the comparator and the decoder. The DS-DFF utilizes a high-speed DFF [34] to
avoid any bandwidth limitation that could occur with conventional DFFs. The DS-DFF synchronizes the encoded data signal \((x/y/z)\) under external clock. The maximum throughput of a PAM transceiver is limited by the latency skew tolerance of the decoder. In the worst case scenario of random bit encoding, there will be an unavoidable latency skew due to the slow rising and falling transitions of each PAM level symbol \((x/y/z)\). This may trigger degraded latency skews of the control signal \((x/y/z)\) and unwanted glitches of the decoder outputs. To mitigate these problems, the proposed DSDFF can sample the encoded PAM signal by synchronizing the edge of the signal transition \((x/y/z)\) to the source-synchronous clock reference. Fig.3.12 shows the schematic of the DS-DFF.

![Fig.3.12 DFF circuit used in PAM receiver](image)

The proposed PAM receiver also includes a digitally controlled on-die-termination (ODT) logic that can adjust and match the input impedance of the PAM receiver to the characteristic impedance of the off-chip transmission line. Typically, the on-chip resistance on a CMOS technology has a significant process variation of resistance (ex. \(-25\%\text{ to }+25\%\) of a polycrystalline resistor). Therefore, the digital controlled ODT termination circuits can help improve signal integrities by minimizing the signal reflection. Fig.3.13 shows the schematic of the digital control ODT.
3.5. Design of PAM Transceiver

The 4-level PAM I/O memory interface is designed in 65nm CMOS technology shown in Fig.3.14. It achieved an overall data rate of 8Gb/s under chip testing. This performance is much improved than that of conventional memory interfaces [48]–[52]. This PAM level can be further extended to more levels in the future, such that more data streams can be carried with much improved energy efficiency. Fig.3.15 shows the output eye diagrams of the PAM receiver.
Normally for PAM transceivers, output data eye diagrams are degraded due to noises from multiple reference voltage level. However, due to dual sampling structure in this design, the PAM transceivers’ eye diagrams do not show severe distortion which normally appears in conventional PAM transceivers.

A set of MATLAB code was made to plot the constellation of input 4-PAM signal of the receiver. Fig.3.16 shows the 4-PAM constellation. Each level is clearly separated so that it is possible for the receiver to recover the original signal.
Fig. 3.16 Constellation of 4-PAM signal (a) 4-PAM constellation (b) constellation of each level
CHAPTER 4

DESIGN OF ON-CHIP BAND-SELECT TRANSFORMER

4.1. Introduction

This chapter will cover the design flow of the on-chip band-select transformer for signal splitting at RF-band receiver. Also the RF-bands cannot be resistively terminated and instead require a transformer. Therefore the band-select transformer is critical in MMI system because it acts as an impedance matching circuit that couples the signal of RF transmitters to transmission line while decouples the signal for the RF receivers. The idea of band-select transformer is developed from a prototype research work as demonstrated in [5]. The Dual Band Interface (DBI) uses a single transformer to couple and decouple RF and Baseband signals. In MMI system, two transformers are connected together to form a band-select transformer. However the design needs to be carefully calculated before implementation. The rest of the chapter will demonstrate the design and characterization of the band-select transformer.

4.2. Transformer Impedance Matching in Memory I/O Interface

In the prototype design of DBI in [5], an on-chip transformer with primary-to-secondary-coil turn ratio of 2:1 is chosen. The objective of the transformer is to effectively couple/decouple its RF signal and isolate it from the baseband signal (DC blocking). Furthermore, its purpose is not just for filtering, but also impedance matching of the input impedance of the receiver to the characteristic impedance of the transmission
line as shown in Fig.4.1 (a). Unlike the baseband signaling, the RF-band signal cannot be
terminated by using a simple resistor, since the parasitic around the resistor would
dominate at high frequencies. The transformer is loaded by the mutual-mixer input stage
which the input impedance is modeled by series connection between a resistor and a
capacitor as shown in Fig.4.1 (b). The detailed step-by-step analysis is given in [5]. It
shows that the input impedance seen at the secondary coil in parallel with the input
impedance of the receiver is about 200\(\Omega\) at resonant frequency, which is also the carrier
frequency of ASK signal. Therefore the impedance seen at the primary coil of the
transformer is \(200\Omega/N^2=50\Omega\), which is the basic idea of impedance matching using
transformer. This is idea also applies to the band-select transformer used in MMI, but will
be more complicated in analysis and design.

Fig.4.1 Transformer impedance matching in DBI: (a) schematic of RF receiver in DBI, (b)
lumped model of RF receiver in DBI, (c) impedance matching
4.3. Design of Band-Select Transformer

Band-select transformer plays a very important role in the functionality of the proposed MMI. As indicated in Figure 1.5, the band-select transformer needs to satisfy two major functions in the design. First is to combine the two RF-band signal and baseband PAM signal together into a single stream of mixed signal at the transmitter side. Second is to separate the RF and baseband signal, and send them into their receiver respectively at the receiver side. The second function is more critical for the reason this transformer is named.

![Diagram of band-select transformer](image)

*Fig.4.2 Band-select transformer with RF receivers and their lumped models*

As seen in Fig.4.2, the band-select transformer can be simply considered as merging two regular transformers in [5] together to form a novel three port transformer.
The sizes and inductances of the two regular transformers are different according to different carrier frequencies of MMI. Each regular transformer can be modeled as a balun [55][56][57][58] which converts single ended signal to differential for the differential input of RF receivers. Each regular transformer has a primary to secondary coil turn ratio of 1:2. Each transformer together with its RF receiver serves as a narrow band filter. When looking into the secondary coil of the transformer, an RLC resonant tank is formed with the impedance shown as the dashed line. The real part of the mutual mixer input impedance $R$ is boosted to roughly 200Ω at the resonant frequency. This 200Ohm loading impedance corresponds to an impedance of $200Ω/N^2=50Ω$ impedance reflected at the transformer input side (primary coil), for $N=2$. Therefore by carefully choose the coil inductance $L$ and turn ratio $N$, the band-select transformer can split the input signal to designated components (RF and baseband) for the receivers.

$$Z_1(\omega_{o1}) = \frac{R_1L_1}{Z_1} \frac{R_{S1}}{Z_1} \frac{1}{R_1C_1} = \frac{R_{S1}R_1C_1 + \frac{1}{R_1C_1}}{R_{S1} + R_1} \cong Q^2R_1 = 200 \Omega \quad (3)$$

$$Z_3(\omega_{o1}) \cong \left(\frac{1}{2}\right)^2 \cdot Z_1(\omega_{o1}) = \left(\frac{1}{2}\right)^2 \cdot 200 \Omega = 50\Omega \quad (4)$$

The physical design of the band-select transformer starts with the calculation and simulation of each single transformer. After simulating the input impedance of each RF receiver, the secondary coil inductances of the single transformers are calculated be to 650pH and 1.5nH at 24.6GHz and 12.3GHz respectively. Of course, each single transformer has a turn ratio of 1:2. All momentum simulations of passive devices are performed on ADS [53]. Fig.4.3 shows the 3D view of a single transformer which the inner diameter is 100um.
Fig. 4.3 3D view of the single transformer #1 with inner diameter of 100um

The resonant frequency of single transformer #1 is 24.6GHz. Fig. 4.4 shows the simulation results of the inductance of secondary coil and the k factor of the transformer where $L_1=669\text{pH}$, $k=0.7$. Those values are accurate enough for the design.
Fig. 4.4 Secondary coil inductance and k factor simulation of transformer #1

Fig. 4.5 shows the 3D view of a single transformer which the inner diameter is 1750um.

Fig. 4.5 3D view of the single transformer #2 with inner diameter of 175um

The resonant frequency of single transformer #2 is 12.3GHz. Fig. 4.6 shows the simulation results of the inductance of secondary coil and the k factor of the transformer where $L_1=1.696\text{nH}$, $k=0.8$. 
Fig. 4.6 Secondary coil inductance and k factor simulation of transformer #2

Fig. 4.7 shows the complete layout of the band-select transistor. The two coils are implemented by the top layers M7 and M8 of the PDK.

Fig. 4.7 Layout of three ports band-select transformer

Fig. 4.8 shows 3D view of the band-select transformer in ADS and its s-parameter simulation.
However, considering the high parasitic resistance of on chip transformer in Fig.4.2, the quality factor of the filter is not high enough, making the filter not sharp enough at the two resonant frequencies. Therefore affects the isolation between the two RF bands carriers. This phenomenon could be observed in Fig.4.8 (b), which shows $S_{11}$.
simulation result of impedance seen from $Z_3(\omega)$. The isolation between the two bands is -10.8 dB due to the reason mentioned above. By implementing this band-select transformer into the proposed MMI transceiver, we can achieve filtering at two different frequencies
5.1. Introduction

The comprehension of this chapter covers the analysis, design, layout and chip testing of the proposed MMI system, where integrates all components such as low noise VCO (LNVCO), RF-band transceiver, band-select transformer, and PAM transceiver to support simultaneous data streams on a single-ended shared off-chip transmission line. The MMI transceiver is designed and fabricated in 65nm CMOS technology. The PAM and RF-band transceivers carry 8Gb/s/pin and 6Gb/s/pin, respectively, on a 5cm shared off-chip transmission line. The MMI transceiver operates at 14Gb/s/pin with the power efficiency of 2.8pJ/b.

5.2. MMI Transceiver

Fig.5.1 (a) shows the system architecture for the proposed MMI system. Fig.5.1 (b) shows the intended MMI signaling that contains both 4-PAM baseband and RF-band for multiple concurrent data communications. The proposed MMI system architecture includes two RF-band transceivers (RFTX and RFRX) and a baseband transceiver (PAMTX and PAMBRX) with a single-ended shared off-chip transmission line. These transceivers provide a CPU-memory communication interface which is needed to transmit and receive data and command from both sides. In this system, where BBTX and
BBRX communicate with each other by using a multilevel 4-PAM signaling, and the RFTX and RFRX communicate concurrently by using ASK signaling. Fig.5.1 (b) shows the dual-band frequency allocations for a concurrent I/O interface in frequency domain. The proposed multilevel 4-PAM and RF-band signaling with a synchronous clocking scheme enables to communicate multiple data streams through RF-band and multilevel baseband without any significant latency penalty.

![Diagram](image)

Fig.5.1 Block diagram of MMI with simultaneous bidirectional simulation of four input data streams
Fig. 5.1 (a) also shows the post-extracted simulation waveforms with simultaneous bi-directional four input data streams, represented by D₁ to D₄. The input data D₁ and D₄ is modulated by 12.3GHz and 24.6GHz carrier frequency at their ASK modulator. Baseband signal D₂ and D₃ are modulated into 4-PAM signal. All these signals are combined by the band-select transformer and sent to the transmission line. Finally, after split by the band-select transformer at the receiver side, each stream signals are recovered by the receivers respectively.

5.3. MMI System Post-Layout Simulation

Considering the energy-efficient of MMI transceiver, simplest ASK modulation technique needs to be considered. Figure 6.3 shows the MMI system at CPU side. Two RF-band transmitters and a PAM receiver are included. The RFTX contains a low noise VCO, an ASK modulator and an on-chip band-select transformer with on-die termination (ODT). LNVC0 first generates RF carriers at 12.3GHz and 24.6GHz respectively for the ASK modulators. The input data streams D₁ and D₄ modulate the carrier frequencies by switching on/off TG transistors to complete ASK modulation. The modulated output then will be inductively coupled into a shared transmission line by the on-chip band-select transformer to minimize inter-channel interference (ICI). The ODT is also integrated into band-selective transformer to overcome impedance mismatch. The 4-PAM transmitter is composed of comparators, DFFs, a decoder, and an output driver. The two data streams D₂ and D₃ are recovered at the output.
A multilevel receiver receives the 4-PAM signal from the off-chip transmission line. This signal is compared to three levels of DC reference voltages after being sensed by the comparator. Pre-amplifiers are used to convert the incoming single-ended multilevel signal to differential signal for better noise immunity and to maximize multilevel voltage margins. Finally a decoder converts the output of comparator at each clock cycle into the original output bits.
Since ASK modulation only senses the incoming signal’s amplitude, the power-hungry frequency and phase synchronizations between RF transmitter and receiver are not required. This will greatly simplify the overall mobile interface design and therefore
reduce the overall power consumption of the whole system. Fig.5.3 shows the CPU side layout of the MMI chip.

Fig.5.4 Complete schematic of MMI system at memory side

Fig.5.4 shows the complete schematic of MMI system on memory side. By using the band-select transformer both RF PAM signals are split and sent to their individual receivers. After band-pass filtering from the transformer, the RF-band data stream is then injected to the differential mutual-mixer. A pair of resistor-loaded switching devices and
a class-AB amplifier with resistive feedback can be utilized to further filter out the residue of the unwanted second order harmonic of the RF carrier. The PAM transmitter consists of a DAC-based output driver and an impedance controller. A multilevel control logic circuit creates different output levels by selecting different voltage to the baseband output driver. The level control logic circuit turns on a combination of PMOS and NMOS transistors such that the total output impedance of the output driver would be always same as the characteristic impedance of the transmission line in order to provide output impedance matching. Fig.5.5 shows the layout of the 4-level PAM transmitter and RF-band receivers.
Fig. 5.5 Complete layout of MMI system at memory side: (a) RF receiver, (b) PAM transmitter

The total area of the chip top layout is 1mm by 1mm. The CPU side and memory side are power with separate power pads therefore the chip can be used at both side across the off-chip transmission line.

Fig. 5.6 shows the post-layout simulation waveforms showing simultaneous bidirectional communication of MMI system. Input and output data streams of the RF-band transceiver are shown in Fig. 5.6 (a) and (b). The simulation waveforms of the 4-PAM channel can be viewed in Fig. 5.6 (c) and (d). A limited delay existed between input and output data, because the off-chip transmission line.
Fig. 5.6 Simultaneous bi-directional simulation waveforms under four data input

Fig. 5.7 shows the eye diagrams of all four data outputs. The data rate of both baseband channels are 5Gb/s/pin, making the 4-PAM signal data rate of 10GHz/s/pin. Both RF band data rate is 5Gb/s/pin. Therefore, the proposed MMI transceiver handles 4 data streams simultaneously with a total data rate of 20Gb/s/pin at 1.2V supply voltage. The energy-efficiency of the MMI transceiver in the simulation is 2.8pJ/b.
5.4. FR4 Transmission Line Modeling

The frequency characteristic of the off-chip transmission line on FR-4 PCB is needs to be deeply analyzed since the RF-band signal may seriously degrade at the carrier frequency of more than 20GHz. The physical layer of the transmission line is simulated using ADS. Insertion loss of transmission line under high frequency might delay, disperse, and attenuate the signal. The use of differential transmission lines for RF-band signal can minimize skew and better rejects common-mode noise. However, differential transmission line needs more space and consumes more power. Therefore single-ended transmission line is better preferred nowadays.

Designing a single-ended transmission line for high speed transceiver is very challenging. More high frequency effects needs to be considered compared to low frequency transmission lines. Therefore choosing the geometry of the transmission line is necessary for impedance matching to minimize signal reflections. Considering the random error in PCB fabrication, several width of transmission line will be implemented on PCB board and measured to correlate the ADS simulation results for best performance. The characteristic impedance depends on the width of transmission lines. The impedance decreases with thicker lines, and increases with thinner lines under same substrate. Therefore we choose PCB thickness of 16mil for the test board design according to experimental results.
Fig. 5.8 ADS model of FR4 transmission line with wire bonding

Fig. 5.8 shows ADS models of the off-chip transmission line with wire-bonding. After choosing the size of the PCB trace, the 3D transmission line model was simulated in ADS to generate accurate S-parameter data for 5-cm off-chip channel for MMI system.

Fig. 5.9 shows the simulated signal loss of the 5cm off-chip transmission line. The signal loss of 5cm FR4 transmission line at 24.6GHz is around -5dB.
5.5. MMI Chip Testing

The MMI chip is fabricated in the Global foundry 65nm CMOS process. It demonstrates simultaneous and bi-directional data communication in testing. Fig.5.10 shows the Die Photo of MMI chip under microscope. The chip area is 1mm$^2$.

![Die photo of MMI chip](image)

Fig.5.10 Die photo of MMI chip

Fig.5.11 shows the picture of FR4 testing board with MMI transmitter and receiver mounted on it. Some important design guidelines need to be considered when designing high-speed PCB testing board. A narrow spacing between power and ground can also create an excellent high frequency bypass capacitance. Power and ground pins should be connected to power and ground planes, respectively, with wide low-impedance traces. Surface mount capacitors should be used to minimize high frequency parasitic inductance and should be located close to chip pins.
Fig. 5.11 MMI testing board

Fig. 5.12 shows setup of testing equipment for chip testing. Testing equipment for MMI chip includes: Agilent HP Modular Signal Generator (70340A), Agilent 86100D DCA-X Wide-Bandwidth Oscilloscope, and DC power supplies.

Fig. 5.12 Equipment setup for MMI testing

Four random data streams are generated by PRBS generator which is synchronized by the clock generator. The random data input streams are sent to baseband and RF-band input connectors to demonstrate the simultaneous and bi-directional data communication. The output random data sequences are received and measured by the Agilent 86100A oscilloscope.
Figure 5.13 shows the measured eye diagrams of aggregate 14Gb/s/pin data rate on FR4 test board. Testing results show that the 4-PAM transceiver has total data rate of 8Gb/s, and each RF transceiver has 3Gb/s data rate.

![Eye Diagrams](image)

**Fig. 5.13** Measured output eye diagram of MMI chip (a) RF-band output #1 eye diagram at 3Gb/s/pin (b) RF-band output #2 eye diagram at 3Gb/s/pin (c) 4-PAM output #1 eye diagram at 4Gb/s/pin (d) 4-PAM output #2 eye diagram at 4Gb/s/pin

Worst case eye diagram occurs in Fig.5.13(c), where the eye-open is the smallest. Therefore it is reasonable to calculate worst case bit error rate (BER) of the output data base on eye diagram of Fig.5.13(c). The BER is calculated through Gaussian approximation, which is shown in Eqn.5.1.

$$BER = \frac{1}{2}erfc \left( \frac{1}{\sqrt{2}} \frac{\mu_H - \mu_L}{\sigma_H + \sigma_L} \right)$$
In Eqn.5.1, $\mu_H$ and $\mu_L$ are the mean values, $\sigma_H$ and $\sigma_L$ are the standard deviations of the high and low bit levels respectively. The operator erfc is the complementary error function. As indicated in Fig. 5.14, the BER is essentially the probability of bit error occurs in a certain sample of bits under normal distribution condition, which in the figure is the overlap area of the two normal distribution plots.

![Fig.5.14 Error probability of binary symmetric channel](image)

Since the difference of mean values of high and low $\mu_H-\mu_L$ can be easily observed in the eye diagram, in this case 272.4mV, the problem remaining is how to derive the standard deviations $\sigma_H$ and $\sigma_L$ to complete finish Eqn.5.1. Since the cumulative distribution remains roughly constant with same number of sample in normal contribution, it is reasonable to make a new figure of merit $N_S$, which is defined as:

$$N_S = \frac{S_{max} - S_{min}}{\sigma_S}$$

(5.2)

$S_{max}$ and $S_{min}$ are the maximum and minimum sample values, and $\sigma_S$ is the standard deviation. Number of Sample N in the eye diagram of Fig.5.13 can be calculated
by multiplying the update rate of the oscilloscope and the time of measurement, in this case is 400 waveforms/second and 60 seconds respectively. Therefore number of sample \( N = 400 \times 60 = 24000 \). Fig.5.15 shows the program in which \( N_S \) is calculated under 24000 samples. \( N_S = 8.13 \).

\[
\text{Fig.5.15 Figure of merit calculation}
\]

Therefore \( \sigma_H \) and \( \sigma_L \) can be calculated as:

\[
\sigma_H = \frac{(H_{\text{max}} - H_{\text{min}})}{N_S} = \frac{142.7 \text{mV}}{8.13} = 17.55 \text{mV}
\]

\[
\sigma_L = \frac{(L_{\text{max}} - L_{\text{min}})}{N_S} = \frac{145.9 \text{mV}}{8.13} = 17.95 \text{mV}
\]

According to Eqn.5.1, BER = \( 8.6 \times 10^{-15} \) for the worst case scenario, which meets industrial standards.

Another method to calculate \( \sigma_H \) and \( \sigma_L \) is by collecting the grayscale values of certain pixels in eye diagram image. In this case, 11 pixels are chosen from high and low eye opening linearly across the waveform distribution, as shown in Fig.5.16.

Fig.5.17 shows the grayscale values distribution for both high and low. And calculated \( \sigma_H = 33.25 \), \( \sigma_L = 40.05 \). Therefore the calculated BER = \( 1.5 \times 10^{-7} \).
Fig. 5.16 Grayscale conversion from RGB image

Fig. 5.17 Grayscale values distribution
Table 5.1 compares MMI performance to that of prior memory I/O interfaces. The MMI interface exhibits higher aggregate data throughput (14Gb/s/pin) and better energy efficiency (2.8pJ/b) compared with prior arts.

Table 5.1 Performance Summary and Comparison

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>65nm CMOS</td>
<td>65nm CMOS</td>
<td>40nm CMOS</td>
<td>28nm CMOS</td>
<td>65nm CMOS</td>
</tr>
<tr>
<td># of bands/pin</td>
<td>0.5</td>
<td>2</td>
<td>1</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>T-line length</td>
<td>5mm</td>
<td>5mm</td>
<td>5mm</td>
<td>30mm</td>
<td>5mm</td>
</tr>
<tr>
<td>Data rate</td>
<td>6.25Gb/s/pin</td>
<td>8Gb/s/pin</td>
<td>5Gb/s/pin</td>
<td>3.75Gb/s/pin</td>
<td>14Gb/s/pin</td>
</tr>
<tr>
<td>Direction</td>
<td>Non-bidirectional</td>
<td>*SBD</td>
<td>Non-bidirectional</td>
<td>Non-bidirectional</td>
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Note: *SBD (simultaneous bidirectional)
Chapter 6

CONCLUSIONS AND FUTURE WORKS

6.1. Conclusions

The primary goal of this study has been achieved after 3 years of researching: the design a novel memory I/O interface with high bandwidth and high energy-efficient for mobile computing systems in order to dramatically enhance the circuit and system bandwidth and power efficiency. The proposed memory I/O interface, exploiting multi-modulation and multi-band signaling, is capable of supporting simultaneous bidirectional data transition of 4 separate data streams across a single-ended off-chip transmission line to achieve both high speed data rate and low power consumption. This multi-band multi-modulation interface (MMI) consists of multiple RF-band transceivers which utilize ASK modulation, and baseband transceivers which utilize PAM modulation to increase the I/O bandwidth while supporting simultaneous bidirectional communication. After the ASK and 4-PAM modulation process of each data channel, the 4 data streams are coupled by a novel band-selective transformer into an intermediate mixed signal which consists of both RF and baseband frequencies. This novel band-selective transformer has not been designed before for memory interface. The intermediate mixed signal from the output of the band-selective transformer is then transmitted through the single ended off-chip transmission line into the MMI receiver. Once the secondary coil of the transformer at the receiver side senses the intermediate mixed signal, it filters the out the unwanted RF-band frequency and provides the remaining in-band ASK data into the RF receiver. For
baseband signal, it simply travels through the metal wire of both the transformers coils to the baseband receiver. Therefore, after the modulated signals in each receiver side are demodulated, the original 4 individual input data are then recovered at the output.

The MMI circuit was implemented in 65 nm CMOS process technology. Testing results show that the MMI interface achieves an overall data rate of 14Gb/s/pin and a better energy efficiency of 2.8pJ/b/pin compared to prior works.

This MMI circuit is designed with low power and reconfigurable feathers primarily for future mobile application since mobile device power is limited by the battery technology. Mobile devices like the latest Apple iPhone 8, where the flip-chip micro-bumps were used to connect CPU and RAM, the loss is trivial compared to 5cm on-board transmission line in MMI situation. Therefore MMI could be easily applied to future iPhone products. Further investigations on computer devices also show that the MMI chip can be applied to tablets, laptops, and even desktop computers.
Fig.6.1 shows the internal structure of an Apple iPad. It’s CPU (red) and RAM (yellow) are placed very close to each other with much less than 1cm distance. Therefore if MMI chip is applied to the future products, it will greatly enhance the performance and reduce the number of connections.

![Image of Apple iPad internal structure]

*Fig.6.2 Distance of CPU and DRAM in Apple iMac [60]*

Even for desktop computers like Apple iMac as shown in Fig.6.2, the distance between its CPU and RAM is no longer than 30mm. Therefore even the size of future iMac becomes larger; MMI could still be a good preference to enhance the performance while reducing the overall power.

**6.2. Future Works**

MMI is an initial attempt of utilizing multi-band and multi-modulation technique to achieve simultaneous and bi-directional communication of four data streams on a shared transmission line. After more comprehensive and detailed testing on the reliability
and stability of MMI, new ideas will be developed based on MMI structure to achieve higher performances.

The architecture of the 3D eight-level pulse amplitude modulation (8-PAM) transceiver is shown in Fig.6.1. The 8-PAM transmitter and receiver communicate through 3D micro bump to improve signal integrity. In the 8-PAM transceiver, novel encoder and decoder are utilized to transmit and receive three data streams through a single 3D micro bump.

![Fig.6.3 8-PAM transceiver](image)

With an extra data stream added to the baseband, a new idea will be developed to add one more data stream to the RF-band. This involves the design of a four port band-select transformer as shown in Fig.6.2.
Fig. 6.4 New band-select transformer with four ports

By implementing this new band-select transformer, an extra data stream can be added to the RF-band. On-board transmission line is replaced by micro bumps or TSVs to increase channel bandwidth and signal integrity.
REFERENCES


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[60] https://hothardware.com/