High-Speed Single-Channel SAR ADC Using Coarse and Fine Comparators with Background Comparator Offset Calibration

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HIGH-SPEED SINGLE-CHANNEL SAR ADC USING COARSE AND FINE COMPARATORS WITH BACKGROUND COMPARATOR OFFSET CALIBRATION

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HIGH-SPEED SINGLE-CHANNEL SAR ADC USING
COARSE AND FINE COMPARATORS WITH
BACKGROUND COMPARATOR OFFSET CALIBRATION

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with a
Major in Electrical Engineering

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I would like to thank Prof. Gui for the constant guidance and support throughout this work. I'm also forever grateful to my family for being so patient with me and my friends for supporting me.
A 1-GS/s 8-bit single-channel successive-approximation-register (SAR) analog-to-digital converter (ADC) using coarse and fine comparators with fully background comparator offset calibration is presented. Low-power coarse comparators and low-noise fine comparators are both employed to improve the comparator power efficiency. Non-binary digital-to-analog converter (DAC) with redundancy is employed to tolerate possible errors in the most-significant-bit (MSB) decisions. A novel comparator offset calibration scheme is proposed to remove the offsets between the different comparators, without slowing down the speed of the SAR conversion. The prototype ADC is simulated in a 28 nm CMOS technology and achieves an SNDR of 42.13 dB near Nyquist frequency while consuming 3.2 mW.
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This is dedicated to my parents.
CHAPTER 1

1.1 Introduction

Analog-to-digital converters (ADCs) are one of the most important fundamental building blocks of various application, such as digital communication, audio, video, sensors and control systems. The analog-to-digital (A/D) interface converts a continuous-amplitude, continuous-time signal to a discrete-amplitude, discrete-time signal. Figure 1 shows this interface in more detail. First, an anti-aliasing filter (AAF), which is essentially an analog low-pass filter, is applied to the analog signal to limit its bandwidth, so that the subsequent sampling would not be affected by the aliasing of unwanted noise and signal components. Next, the signal is sampled by a sample and hold circuit (S/H) so that the continuous-time signal becomes a discrete-time signal. Quantization is then applied so that the discrete-time, continuous-amplitude signal is converted into discrete-
time, discrete-amplitude signal. Finally, a digital representation of the signal is produced at the output by the DSP.

![Diagram of Analog-to-Digital Converter](https://example.com/diagram)

**Figure 2.** Basic Analog-to-Digital Converter.

As shown in Figure 2, ADC’s core function is to convert an analog input signal into N-bit digital output signal. The conversion is performed at a certain speed, which is defined as sampling frequency $f_s$. In order to do the work, the ADC needs to burn certain amount of power (P). The relationship between the sampling frequency $f_s$ and input signal bandwidth distinguishes two categories of ADCs. For the Nyquist ADCs, the sample frequency must be at least two times of the input signal bandwidth, so that the original signal can be accurate reproduced without losing any information, according to the Nyquist Theorem. On the other hand, for oversampling ADCs,
the ADCs is operating at a sampling frequency many times of the Nyquist rate. Digital filtering is applied afterwards to remove the noise from outside the band of interest. Noise shaping is often employed to improve the efficiency of filtering. In this dissertation, we mainly focus on the Nyquist rate ADCs.

ADCs with a sampling frequency at gigahertz has a wide application in modern communication systems such as 5G, next generation WiFi, next generation optical communication systems. The gigahertz range high-speed ADCs could be used to digitize RF signals directly, without an analog frequency conversion to a lower Intermediate Frequency (IF) or baseband (Zero IF). These high-speed ADCs are generally called as “RF sampling ADCs”, which can replace a radio signal path subsystem of mixers, LO synthesizers, intermediate frequency amplifiers and filters, reducing bill of materials, cost, design time, size, weight, and power, while increasing the software programmability and flexibility of the system.

1.2 Background

1.2.1 Amplitude Quantization

To change the input signal from continuous-amplitude signal into discrete-amplitude signal, amplitude quantization is required [1]. The dynamic range of the quantizer can be divided into certain number of equal quantization steps, which is represented by a certain analog amplitude.

Assuming that

\[ X_{FS} = X_{max} - X_{min} \]  

(1.1)

\( X_{FS} \) is the full scale range of the quantizer, the amplitude of each quantization interval or quantization step \( \Delta \) is

\[ \Delta = X_{FS}/M \]  

(1.2)
where M is the number of quantization intervals. Since the mid point of the n-th interval

\[ X_{m,n} = (n + 1/2)\Delta \]  

(1.3)

which represents all the interval amplitudes, quantizing an input level other than \( X_{m,n} \) causes an error. This is called the quantization error, \( \varepsilon_Q \). The output \( Y \) of a quantizer with input \( X_{in} \) is

\[ Y = X_{in} + \varepsilon_Q = (n + 1/2)\Delta \]  

(1.4)

Figure 3. Quantization error added to the input signal obtains the quantized output
Figure 3 depicts the quantization process: the quantization error $\varepsilon_Q$ is added to the input to produce the quantized output. The addition is a linear operation but the added term is a non-linear function of the input. Figure 3 plots the quantization error $\varepsilon_Q$ for an ideal 3-bit quantizer. The maximum value of the quantization error $\varepsilon_Q$ is $\Delta/2$.

We can also represent the quantization interval by a digital code instead of identifying a quantization interval by its mid-point. In this case, the output is represented by a digital word instead of a discrete analog level. The number of quantization intervals is usually a power of 2, such as $2^N$, where $N$ is the number of bit. Thus, for the example of Figure 4, we can use a decimal symbol from 0 to 7 or a binary 3-bit code to represent those analog values.

![Figure 4. Quantization error for a 3-bit quantizer](image)

1.2.2 Quantization noise

The previous section shows that quantization leads to the addition of quantization error and input signal. A large quantization error leads to poor signal quality. We can borrow the Signal-to-
Noise Ratio (SNR) concept here. In the case where electronic noise corrupts an analog signal, the effect of noise is quantified by SNR, which is defined as

\[
\text{SNR}_{dB} = 10 \cdot \log \frac{P_{\text{sig}}}{P_{\text{noise}}},
\]

where \( P_{\text{sig}} \) and \( P_{\text{noise}} \) are the power of the desired signal and power of electronic noise in the band of interest, respectively.

It is quite convenient to use the SNR concept when analyzing the effect of quantization error. However, this statement is only true when the quantization error can be regarded as noise. Some input signals can lead to a quantization error other than noise. For example, a DC signal simply leads to a constant quantization error. Also, when the frequency of the input signal is integer multiples of the sampling frequency, the quantization error would not look like noise. On the other hand, signals that cause recurrent crossing of quantization threshold works well. Frequency code transitions decorrelate input signal and quantization error, thus spreading the spectrum and making the quantization error look like noise. Therefore, signals with large busy amplitudes are promising candidates for the desired noise-like representation.

The above qualitative discussion is formally specified by the following set of necessary conditions:

1. All the quantization levels are used with same possibility;
2. Most quantization levels are exercised;
3. Uniformed quantization intervals;
4. No correlation between the input and the quantization error.
Figure 5. Quantized signal and quantization error.

The first requirement can be met by employing large input signal.
The second requirement can be met when the quantizer uses a large number of bits, which is valid in most scenarios. However, for sigma-delta ADCs, which is a very important type of ADCs uses very few quantization levels, just two levels usually: 1-bit. Thus, for sigma-delta ADCs the second requirement for the quantization to be additive noise is not well justified. Still, designers employ the noise approximation anyway, since the noise approximation provide good intuitive insight for circuit designers.

The third requirement can be met by most quantizers. Even the last requirement can be met in most cases. However, if a sine wave is fed into a data converter, which is often the case in ADC testing. The frequency of the input needs to be chosen carefully. If the ratio between input frequency and the sampling frequency is a rational number, the quantization noise will be correlated with the input signal.

Figure 5 shows a 10-bit quantized signal and its quantization noise. The ratio f_s/f_in is 150. Observe that the signal swing is in the range of ±1, and the quantization error is in the range of ±1/1024. Also, the error shows a periodic pattern. The correlation between the inputs and the quantization error suggest that when performing a single tone sine wave test, the input frequency must be carefully chosen.

\[
\text{SNR}_{dB} = 10 \cdot \log \frac{P_{\text{sig}}}{P_{\text{noise}}},
\]  

(1.6)

1.2.3 Property of Quantization noise

The noise spectrum and time average power is two critical properties for any type of noise. The property of noise power in frequency domain is shown in the noise spectrum. The spectrum
of quantization noise is only meaningful in the Nyquist frequency, since it is associated with a sampled-data signal.

Estimating the time average power of the quantization error assumes a constant probability distribution function $p(\varepsilon_Q)$ in the range of $\pm \Delta/2$ and $p(\varepsilon_Q)$ is zero outside this range. The first condition given in the previous sub-section justifies this assumption. Moreover, $|\varepsilon_Q|$ is always less than $\Delta/2$. Since the integral of the probability distribution function over the infinite range is equal to one, it leads to

$$p(\varepsilon_Q) = \frac{1}{\Delta} \text{ for } \varepsilon_Q \in \left(-\frac{\Delta}{2}, \frac{\Delta}{2}\right),$$

$$p(\varepsilon_Q) = 0 \text{ otherwise}, \quad (1.7)$$

The time average power of $\varepsilon_Q$ is given by

$$P_Q = \int_{-\infty}^{\infty} \varepsilon_Q^2 \cdot p(\varepsilon_Q) d\varepsilon_Q = \Delta^2/12. \quad (1.8)$$

As expected, as we increase the number of bits, the time average power of the quantization noise decreases. Furthermore, it is proportional to the square of LSB size. The use of (1.8) and the power of the signal enable us to calculate the SNR. If we assume the input signal is sine wave, since the maximum amplitude of a sine wave within an $X_{FS}$ dynamic range is $X_{FS}/2$, the power of the sine wave is

$$P_{sin} = \frac{1}{T} \int_{0}^{T} \frac{X_{FS}^2}{4} \sin^2(2\pi ft) dt = \frac{X_{FS}^2}{8} = \frac{(\Delta 2^n)^2}{8}. \quad (1.9)$$

Therefore, (1.8) and (1.9) lead to

$$SNR_{sine, dB} = (6.02n + 1.78) dB \quad (1.10)$$
Equations (1.10) gives useful relationship between the maximum achievable SNR and the number of bits of a quantizer. We can see that resolution of a quantizer improves the SNR by 6.02 dB when number of bits is increase by 1. Also, the power of the quantization noise diminishes by a factor 4 when number of bits is increase by 1.

The SNR calculation we showed above only accounts for the quantization noise. In reality, components such as transistor, resister, etc., always introduce additional noise to the circuits. Also, signal distortion is inevitable.

The above SNR calculation only accounts for the quantization noise. In real circuits the electronic noise of passive and active components brings about additional noise. The above observations make the noise a more comprehensive limit affecting a real data converter. This is the reason why equation (1.11) is often used more extensively for defining the equivalent number of bits (ENOB). For sine wave input we have

\[ ENOB = \frac{(SNR_{tot,dB} - 1.78)}{6.02} \]  

(1.11)

where \( SNR_{tot} \) is the signal-to-noise ratio accounting for the total noise that affects the signal band of the conversion system.
1.3 Comparison between different ADC Architectures

Figure 6 shows the ADC structures used for different speed and resolution. Conventionally, Successive Approximation Register (SAR) is a typical structure for ADCs with medium speed and medium resolution. However, in the past decade, SAR ADC is becoming one of the most popular structure, even in high-speed ADC designs. Several important merits of the SAR ADC architecture make it an ideal candidate for modern CMOS designs. First, since most of the circuits in a SAR ADC are digital switches, no static current is consumed by the SAR ADCs, as long as the comparator is a dynamic one. This translates into excellent power efficiency comparing to other ADC architectures. Second, SAR ADC gains huge advantage as technology advances, since advanced technology provides smaller and faster transistors with lower intrinsic gain. For SAR ADC, there is no gain stage, so the low intrinsic gain does not impact a SAR ADC while faster transistor increases the conversion speed of the SAR ADC. In addition, several techniques have been proposed to further increase the conversion speed of SAR ADC, as will be discussed in Chapter 2.
Figure 6. Conventional ADC structures for different speed and resolution.

Figure 7 shows the plot of sampling frequency versus signal to noise and distortion ratio (SNDR) of recently published ADCs in International Solid State Circuits Conference (ISSCC) and Symposium on Very Large Scale Integrated Circuits (VLSIC). X axis is the SNDR achieved and the Y axis is the sample frequency achieved. The data points of SAR designs are shown with triangular shapes. As we can see from the figure, SAR is quite versatile in terms of both sampling frequency and resolution. The sampling frequency of the SAR ADC designs covered a range from a few KHz all the way up to 90 GHz. And the SNDR(resolution) of SAR SAR ADC designs covered a range from 25 dB up to 80 dB. While other type of ADCs usually only covers a limited range of speed and resolution. For example, the flash ADCs are for low-resolution high-speed designs and sigma delta ADCs are for high-resolution low speed designs.
Figure 7. ADC Speed versus Resolution.

Figure 8. ADC power efficiency versus resolution.

Figure 8 shows the power efficiency of different type of ADCs. Y axis is the the ratio between the power consumption and sampling frequency and X axis is the SNDR achieved. As we see from
the figure, SAR ADCs proves to be the most power efficient architecture for medium resolution ADCs.

The overview of the dissertation is as follows. Chapter 1 gives a brief introduction and background on data converters. Chapter 2 covers the principal and architecture of SAR ADC. Chapter 3 shows the proposed SAR architecture. Chapter 4 shows the detailed implementation of proposed SAR ADC. Chapter 5 gives the measurement result. Chapter 6 draws the conclusion.
2.1 Binary Search Algorithm

Conventional SAR ADCs use a binary search algorithm to convert analog signal to digital signal. It is shown in Figure 9 how the binary search works. The search range is full signal swing, from 0 to $V_{FS}$. In the first step, we compare the input signal with middle point of the search range, setting the decision level to $V_{FS}/2$. If the input signal is larger than $V_{FS}/2$, the digital output is 1 and the next decision level set to $V_{FS}/2 + V_{FS}/4$. If the input signal is smaller than $V_{FS}/2$, the digital output is 0 and the next decision level set to $V_{FS}/2 - V_{FS}/4$. In the second step, we compare the input signal with $V_{FS}/2 + V_{FS}/4$ or $V_{FS}/2 - V_{FS}/4$, based on the previous bit decision. This process is repeated until all the bits are resolved and we finally get the digitized value of the input signal.

Figure 9. Binary search algorithm
2.2 SAR Architecture

In this section, we will explain the architecture of SAR ADCs and illustrate how the algorithm is implemented.

As showed in Figure 10, the SAR ADCs consist of three blocks. The comparator compares \( V_{in} \) with DAC output voltage. The shift register stores the output of the comparator and control the DAC, which provides proper decision level for the comparator. In addition, a sample and hold circuit is often used to hold the input signal.

![SAR ADC Block Diagram](image)

**Figure 10.** Block diagram of SAR ADC.

In 1975, J. L. McCreary and P. R. Gray proposed the first SAR ADC [9]. It combines the sample and hold circuit with the DAC and the subtraction is performed in the charge domain.
A four-bit binary-weighted SAR ADC based on charge redistribution is shown in Figure 11. One complete conversion takes a sample phase and a conversion phase. A sampled analog signal is usually quantized into N digital bit in N+1 clock cycle.

Next, we will explain how the circuit works. During the sample phase, when \( \phi_1 \) is high, the summing node is grounded and the bottom plates of all the capacitors are connected to the input. The input is sampled on to the capacitors in the charge domain.

![Schematic of a charge-redistribution-based SAR ADC](image)

**Figure 11. Schematic of a charge-redistribution-based SAR ADC.**

\[
Q_x = -V_{in}C_{tot}
\]  

(2.1)

Where \( C_{tot} = 8C + 4C + 2C + C + C = 16C \).
In the first quantization step, as shown in Figure 12, the bottom plate of the MSB capacitor is connected to $V_R$ and all the other capacitors are connected to ground. Now the charge on summing node $Q_x$ can be represented by $V_x$,

$$Q_x = (V_R - V_x) \cdot 8C - V_x (4C + 2C + C + C)$$

(2.2)

Based on charge reservation, we can solve $V_x$ by Equation (2.1) and (2.2).

$$V_x = \frac{V_R \cdot 8C - V_{in} \cdot 16C}{16C} = \frac{V_R - V_{in}}{2}$$

(2.3)

If $V_x < 0$, then $V_{in} > \frac{V_R}{2}$, and MSB = 1, 8C remains connected to $V_R$. If $V_x > 0$, then $V_{in} < \frac{V_R}{2}$, and MSB = 0, 8C is switched to ground.
In the second quantization step, we connect 8C to $V_R$ or ground according to the MSB decision. In the meantime, the 4C is connected to $V_R$, and the rest capacitors are connected to ground, as shown in Figure 13. The comparator then makes the decision of MSB-1. This quantization process is iterated from the MSB to LSB, thus the analog signal is quantized into digital signal.

![Figure 13. Second quantization step (MSB-1).](image)

Note that the voltage at the summing node $V_x$ approaches zero in the end of the quantization process as shown in Figure 14. This leads to an important advantage of the SAR architecture, it is stray-insensitive. The parasitic capacitance at the summing node cannot change the polarity of the summing node voltage $V_x$, it can only attenuate the value of $V_x$. Therefore, the comparator would not be making wrong decisions because of the parasitic capacitance at the summing node, thus the linearity of the output signal would not be degraded.
In actually circuit implementation, the SAR is usually implemented in a differential fashion as shown in Figure 15. The signals before the comparators are in analog domain, so differential signaling is preferred to suppress common mode noise and interference.

![Figure 14. Voltage at the summing node.](image)

![Figure 15. block diagram of differential SAR ADC](image)
2.3 Advantages of the SAR Architecture

Power efficiency is the most important advantage of SAR ADCs. SAR ADCs are power efficient for the following reasons,

- No amplifier is needed for precision amplification of analog signals
- The capacitive DAC consume only dynamic power but no static power
- Only one comparator is needed.

In addition, SAR ADCs are highly compatible with technology scaling. In scaled technologies, transistors have lower intrinsic gain but higher transit frequency. Consequently, the precision amplification is more difficult, but the quality of switching is upgraded. SAR ADCs, being switching intensive and free of precision amplification, directly benefit from the technology scaling.

The same capacitor array is used for sampling the input signal and for implementing the DAC to estimate the input. Therefore, separate sample and hold circuit and DAC is not required, thus design complexity is reduced.

SAR ADCs usually handle a rail-to-rail input signal swing, because no precision amplification is required. With same signal to noise ratio specifications, we can tolerate more noise for a specific application. We can always trade that for speed or power consumption.
2.4 High-Speed SAR Techniques

Various techniques to improve the conversion speed of SAR ADC have been proposed in recent years. A few of the most effective techniques are discussed in the following paragraph.

2.4.1 Asynchronous SAR

![Timing diagram for synchronous SAR](image)

Figure 16. Timing diagram for synchronous SAR

The conventional implementation of the SA algorithm, such as an SAR converter, relies on a synchronous clock to divide the time into a signal tracking phase and conversion phase which progresses from the MSB to the LSB as shown in Figure 16. For an N-bit converter with conversion rate of $F_s$, a synchronous approach would require a clock running at least $(N+1)F_s$. Since an SAR converter is traditionally used in lower conversion rate regime, clock generation is less of an issue. However, for a high-speed converter, the clock generation of this high-speed internal clock is a significant overhead. For example, a 300-MS/s 6-bit SAR would require a 2.1-GHz clock. Synthesizing such a high-frequency clock plus the clock distribution network would likely consume more power than the ADC itself. From a speed perspective, every clock cycle has to tolerate the worst case comparison time, which is composed of maximum DAC settling time and comparator resolving time depending on the minimum resolvable input level. In addition, every
clock cycle requires margin for the clock jitter which will either slow down the conversion speed or impose a stringent jitter requirement on the clock generator.

Therefore, the power and speed limitations of a synchronous SA design come largely from the high-speed internal clock. Using asynchronous [10] processing of the internal comparisons removes the need for such a clock and substantially improves the power efficiency compared to a synchronous design. On the top level, a global clock running at the sample rate is still used for uniform sampling, since most of the digital baseband to date remains in a synchronous world. The concept of asynchronous processing is to trigger the internal comparison from MSB to LSB like dominoes. As shown in Figure. 17, whenever the current comparison is complete, a ready signal is generated to trigger the following comparison.

Figure. 17. Timing diagram of asynchronous SAR ADC.
In the asynchronous SAR approach bit decision time is no longer fixed by the worst case comparator resolving time. The voltage difference ($V_{\text{res}}$) between input signal and reference level determines the comparator resolving time. The worst case comparator resolving time happens when the $V_{\text{res}}$ falls within $\frac{1}{2}$ LSB. The asynchronous conversion takes the advantage of the faster bit decision cycles, since only one of the $V_{\text{res}}$ will fall within $1/2$ LSB due to the successive approximation algorithm. In addition, the high speed internal clock is removed. The prototype design in [10] achieved 600 MS/s using 0.13um technology.

2.4.2 Loop unrolled SAR

The loop unrolled SAR is proposed in [11] to further push the conversion speed of SAR ADCs, as shown in Figure. 18. Unlike a conventional architecture that uses a single comparator followed by digital logic to determine, store, and transfer the comparison results, this architecture uses $N$ comparators for $N$-bit conversion, storing each comparison result into the digital output of each comparator. These digital outputs are utilized simultaneously in two parallel paths: one is directly
to the capacitive DAC, such that the DAC can respond to the results promptly and generate the successively approximated analog signal quickly without being delayed by any digital logic; the other is to a digital clock generator that detects the completion of the current quantization and then generates a “ready” signal to clock the next quantization.

Speed is greatly improved in this approach, however, comparator offsets between the different comparator is a potential issue. In the prototype design the comparator offset is calibrated in foreground mode, which will not track Process-Voltage-Temperature (PVT) variations.

2.4.3 SAR with alternating comparators

Figure 19. Schematic of SAR with alternating comparators.
The SAR architecture with alternating comparators are proposed in [12], as shown in Figure. 19. Adopting the asynchronous approach, this architecture employs two alternating comparator, so that the reset time of the comparator can be eliminated from the SAR timing budget. The offsets between the two comparators is calibrated in background. This calibration method tracks PVT variations, however, a dedicated calibration cycle is needed in the SAR timing budget, which slows down the conversion speed.

2.4.4 Pipelined SAR

![Figure. 20. Block diagram of pipelined SAR.](image)

Besides optimizing the conversion speed of a single stage SAR ADC, pipelining can be employed to further increase the throughput of the SAR[12]-[15]. With an advanced technology such as 14nm, pipeline SAR architecture is proved to be able to run up to 1.5 GS/s at a power consumption of only 7 mW and achieving an SNDR of 50dB [12]. A typical configuration involves two moderate SAR ADCs connected by a residue amplifier, as shown in Figure. 20.
While the overall architecture is pipeline, a few characteristics of this approach are unique to SAR and deserve to be mentioned. First, a large first-stage resolution can be easily attained in a pipelined SAR with a low power overhead. It is widely known that a large front-end resolution helps relax the DAC matching requirement and the residue amplifier settling accuracy. Once a large number of bits are resolved in the first stage, the power consumption of the residue amplifier can be minimized due to much relaxed noise specs on the residue voltage. Secondly, since the input is sampled on the same capacitor array to perform the SAR comparisons and residue transfer to the second stage, no front-end clock skew issue exists in a pipelined SAR. Thirdly, once an inter-stage residue gain is provided, the stringent noise constraint on the second-stage comparator is relaxed for high-resolution applications, which contrasts dramatically to a conventional SAR that requires the comparator to be extremely low noise for at least a few LSB comparisons.

As shown in the timing diagram, the ADC conversion starts with the sampling phase of the first stage SAR. Then the first stage SAR makes six conversions sequentially. After the first stage finishes its last conversion. It triggers the clock of the residue amplifier, which amplifies the
residue voltage and send it to the second stage SAR for further processing. After the residue amplification, the first stage SAR will reset its DAC and begins to sample the next input voltage while the second stage SAR resolves the rest of the bits. Extra bit is usually introduced to implement redundancy, so that the errors from comparator noise and offsets in the first stage SAR can be tolerated.

2.4.5 Time-interleaving SAR

Figure. 22. Conceptual diagram of time-interleaved ADC.
Time-interleaving technique can increasing the speed of SAR ADCs significantly. The block diagram of a conceptual N-way time-interleaved ADC array is shown in Figure. 22, the idea is to put multiple channels of SAR ADCs in parallel. The different channels SAR ADCs sample the input signal at different time instance (ideally with evenly spaced time intervals). However, power consumption increases with the number of channel that was employed and the front-end interleaving circuitry. One inherent drawback of the analog parallelism in a time-interleaved ADC array is channel mismatch, which has limited the performance of this conversion architecture all along. Typical mismatch errors include offset, gain, linearity, and sampling skew mismatch errors. Analog or digital calibration method can be applied to alleviate the channel mismatch problems.

2.5 SAR Power consumption

Previous works mainly aiming at pushing the conversion speed of the SAR architecture, however, the power consumption of the SAR architecture is not carefully optimized.

In terms of power consumption, the three key blocks dominate, which are the SAR logic, the DAC and the comparators. The power consumption of the SAR logic is closely related to technology and conversion rate, so there is limited design freedom for circuit designers. DAC could potentially consume large power, since the total DAC capacitance scales exponentially with resolution. Fortunately, extremely small(sub-fF) unit capacitance is achievable in modern technologies[16]. The potential mismatches of the capacitors due to small size could be corrected using various calibration method [17]-[19]. A unit capacitor as small as 50aF is reported in [20], as the DAC is sized to the thermal noise limit. Furthermore, various DAC switching method have been proposed to optimize the power consumption of the DAC switching activity[21]-[23]. As a result, the DAC only consumes moderate power in well-designed SAR ADCs.
However, the power consumption of the comparators does not benefit from technology scaling. Instead, the comparator noise becomes even worse with scaled supply voltages. Nevertheless, several techniques have been proposed to reduce the comparator power consumption in a SAR architecture. In [24], a noise tolerant SAR was proposed, where two comparators with different input referred noise (IRN) were employed to improve power efficiency of comparators. However, this approach required a binary DAC without any redundancy, which is not always affordable in a typical high-speed SAR since DAC redundancy is required for tolerating the DAC settling errors. In [25], a data-driven noise reduction technique was proposed to reduce comparator power by majority voting for critical decisions. This approach slowed down the SAR conversion process significantly, because multiple comparisons were performed in a sequential manner when the critical bit was detected. In [26], an oscillator collapse-based comparator was proposed, where the comparator could adaptively change its IRN according to the comparator input. However, the oscillator collapse-based comparator operated at a lower speed than conventional strong-ARM or double-tail comparators, thus slowing down the SAR conversion process, too. Therefore, all these techniques are only applicable to relatively low-speed ADC design. Reducing and optimizing comparator power consumptions for high-speed SAR ADCs operating at GS/s sampling rate remains to be a challenging task.
CHAPTER 3

3.1 Overview of the Proposed SAR ADC

The proposed asynchronous SAR ADC architecture is depicted in Figure 23. Coarse and fine comparators with different IRN are employed in order to perform the bit decision efficiently. In addition, two identical comparators are employed in each of the coarse and fine stage so that the two identical ones operate in an alternating fashion [12]. This way the comparator reset time is eliminated from the SAR critical path and the conversion speed increases. The input is sampled to the capacitive DAC via top-plate sampling, so that the MSB decision can be performed.

Figure 23. Block diagram of the proposed ADC.
conveniently without switching any DAC elements. Asynchronous SAR logic [10] is employed in our design to maximize the conversion speed. The DAC is implemented with redundancy to tolerate the DAC settling errors as well as the potential errors made by the coarse comparators during the MSB decisions. A reference comparator is employed to calibrate the offsets of different comparators.

### 3.2 Coarse and Fine Comparators

The noise tolerant SAR proposed in [24] employed a coarse comparator for MSB decisions and a fine comparator for only the last two LSB decisions. Digital correction was performed when the last two LSB decisions showed consecutive zeros or ones. The strategy behind this approach is that if the comparator noise is properly sized, at most 2 out of N comparisons during the SAR operation are likely to be critical because of thermal noise. However, this statement is only true for SAR ADC with binary weighted DAC, which does not have any redundancy. For high-speed SAR ADCs, waiting for the complete settling of the DAC is not always affordable, thus having some redundancy in the DAC is necessary so that some DAC settling errors can be tolerated. This paper proposes a coarse and fine comparator approach with a redundant DAC to tolerate both the coarse comparator errors and the DAC settling errors.

A methodology of optimizing the power consumption of the coarse and fine comparators is shown as following. Assume the energy per comparison of the coarse comparator is scaled down by a factor of k, compared to that of the fine comparator,

\[ E_{\text{coarse}} = \frac{E_{\text{fine}}}{k} \]  

(2.1)

where \( E_{\text{coarse}} \) is the averaged energy consumed by the coarse comparator per comparison and \( E_{\text{fine}} \) is the averaged energy consumed by the fine comparator per comparison. The total power
consumption of the comparators when the coarse and fine comparators are employed can be expressed as

\[ E_{tot} = E_{fine} \cdot M + \frac{E_{fine}}{k} \cdot (N - M), \]  

(2.2)

where \( N \) is the total number of the bit cycles of the SAR and \( M \) is the number of the bit cycles that employ the fine comparators. The total energy consumed by the comparators in the conventional approach is

\[ E'_{tot} = E_{fine} \cdot N, \]  

(2.3)

Combining (2) and (3) yields

\[ \frac{E_{tot}}{E'_{tot}} = \frac{M}{N} + \frac{1}{k} \cdot \left( 1 - \frac{M}{N} \right), \]  

(2.4)

In our design, the IRN of the fine comparator is sized to be the same as the quantization noise power, which gives

\[ \overline{V_{n, fine}^2} = \Delta^2 / 12, \]  

(2.5)

where \( \Delta \) is the LSB size. As we scale down the energy consumed by the coarse comparator by a factor of \( k \), we assume that the IRN of the coarse comparator is scaled up by \( k \) as shown in (6).

\[ \overline{V_{n, coarse}^2} = k \cdot \overline{V_{n, fine}^2} = k \cdot \Delta^2 / 12, \]  

(2.6)

Assuming one redundant bit is inserted during the SAR operation, the maximum redundancy \( (R_{max}) \) that can be achieved is related to the number of decision cycles \( (M) \) that are performed by the fine comparator, which is given in (7),

\[ R_{max} = 2^{M-2} \cdot \Delta \]  

(2.7)
Assuming the comparator IRN follows Gaussian distribution, the redundancy for tolerating the comparator errors needs to be larger than the $3\sigma$ range of the coarse comparator IRN as shown in (8), so that the errors made by the coarse comparator can be corrected.

$$F \cdot R_{\text{max}} > 3 \cdot \sqrt{k \cdot \Delta^2/12}$$

(2.8)

where $F$ ($1 \geq F \geq 0$) is a number that indicates how much of the maximum redundancy is allocated for correcting errors made by the coarse comparators. $F$ is introduced in (8) because the redundancy is also used to tolerate the DAC settling errors, which can be calculated as in [12]. In our design, we set $F = 0.25$ as most of the redundancy is allocated to tolerate the DAC settling errors at a sampling rate of 1 GS/s. Combining (7) and (8) yields $k$ as

$$k < F^2 \cdot 4^M/12$$

(2.9)

Figure. 24. 3-D plot for finding optimum $M$ and $k$
The optimum value of M and k can be found by making a 3-D plot using (4) and (9) in Matlab. Figure. 24 shows a 3-D plot for finding the optimum M and k. In this example, N = 9 and F = 0.25. Since M must be an integer, the resulting plot shows that for minimum power consumption, M = 5 and k = 5.33, resulting a total comparator energy saving of 31.1%.

3.3 Background Comparator Offset Calibration

A novel background comparator offset calibration method is proposed in this paper by using a reference comparator operating in parallel with the other comparators. The reference comparator is implemented with same IRN as the coarse comparators. The calibration scheme operates fully in the background and does not require dedicated calibration time during the conversion. Essentially, the idea is to align the offsets of the four comparators in the proposed SAR architecture to that of the reference comparator. The reference comparator is activated at certain points during the SAR normal conversion as shown in Figure. 25, so that the reference comparator and the comparators under calibration make decisions on the same DAC output.

Figure. 25. Timing diagram of the proposed SAR.
As shown in the timing diagram in Figure. 25, signals “ck1” and “ck2” are the clocks for the coarse comparators; signals “ck3” and “ck4” are for the fine comparators and signal “ck5” is for the reference comparator. Signal “cks” is the sampling clock and signal “cres” is the DAC reset signal. During the conversion of the even input samples, e.g. S2 and S4, the reference comparator shorts its input and performs self-calibration. Although the offset calibration of the reference comparator is optional, it is still performed in our ADC to avoid any systematic offset. During the conversion of the odd input samples, e.g. S1 and S3, the reference comparator is stroked at the 7th bit and the 8th bit decisions, alternatively, performing the offset calibration.

![Comparator input range](image-url)

**Figure. 26. Effective comparator input range for offset calibration**

As shown in Figure. 26, assume that the offset of the reference comparator and the comparator under calibration is OS1 and OS2, respectively. When the comparator input signal falls in region 1 and region 3, the two comparators will output the same results and no information is available for calibration. When the input signal falls in region 2, useful information can be extracted for
calibration. The LSB decisions are statistically better for extracting calibration information. In our design, the 7th bit and the 8th bit instead of the 9th bit are chosen to performed offset calibration, because the 9th bit decision is very close to the DAC reset cycle and would affect the calibration accuracy.

As shown from the timing diagram, the reference comparator operates in parallel with those comparators in the SAR loop, thus no extra calibration time is needed during the SAR conversion. Note that the two coarse comparators are activated during the 7th bit or the 8th bit for calibration, which cost some extra power. Nevertheless, because of the low-power nature of the coarse comparators, this extra power consumption is almost negligible (approximately 1.7% of the total comparator power consumption). On the other hand, the low-noise fine comparators do not need to be activated for an extra cycle for calibration, which saves power consumption.

Since the reference comparator is disconnected from the summing node at every other sample to perform the self-calibration, the summing node sees a time-varying parasitic capacitance, which could lead to dynamic errors. To solve this problem, a dummy comparator is connected to the summing node when the reference comparator is disconnected. This way the time-varying parasitic capacitance is reduced to the input capacitance mismatch between the dummy comparator and the reference comparator, which causes negligible errors according to simulation results.

The clock signals (the 7th bit and the 8th bit clocks) controlling the calibration are readily available internally in the SAR logics. Simple control logics are employed to select the correct "cal" clock and send it to the reference comparator and coarse comparator. Careful layout makes sure the alignment of the calibration clocks. Some slight misalignment is tolerable, because the comparators see a constant input signal being held, not a changing input signal.
With the help of the reference comparator, the offset information of all the comparators can be extracted. These information is then translated into an analog control voltage through digital processing and control DACs. Detailed implementation of these circuitry is described in Chapter 4.

Figure 27. First stage of the comparator
The offset control voltage is connected to the gate of the calibration pair as shown in Figure. 27. With the extra calibration pair, additional noise current is injected into the drain of the comparator input pair. The noise current for the single-end case can be express as

\[
\bar{I}_{n,\text{cal}}^2 = 4kT\gamma g_{m2} + \bar{V}_{n,\text{ctrl}}^2 \cdot g_{m2}^2,
\]  \hspace{1cm} (2.10)

The first term is the intrinsic noise current of the calibration pair. The second term is introduced by the noisy control voltage at the gate of M2 and M3, which represents the noise coming from the calibration loop and we assume it to be \(\bar{V}_{n,\text{ctrl}}^2\). From (10), the IRN of comparators due to the calibration can be calculated as

\[
\bar{V}_{n,\text{cal}}^2 = 4kT\gamma \frac{g_{m2}}{g_{m5}} + \bar{V}_{n,\text{ctrl}}^2 \cdot \frac{g_{m2}^2}{g_{m5}^2},
\]  \hspace{1cm} (2.11)

For noise consideration, \(g_{m2}\) should be minimized, but it needs to be large enough to cover the offset range, since reducing \(g_{m2}\) leads to smaller calibration range. On the other hand, the noise of the control voltage \(\bar{V}_{n,\text{ctrl}}^2\) can be minimized in the digital domain. The comparator output is recorded and the control voltage is updated every N cycles instead of every cycle. This effectively filters out some of the noise in the digital domain. The selection of N provides a tradeoff between convergence speed and convergence accuracy.

The behavioral simulation is performed to demonstrate the effect when different values of N is chosen, as shown in Fig. 6. When the control voltage is updated every 64 samples, the noise (\(V_{n,\text{rms}}\)) on the control voltage is reduce by about 47%, compared to the case where the control voltage is updated every sample. The number of the samples required for convergence is about 11,000 for N = 64. With a sample rate of 1 GS/s, this translates into 11 \(\mu\)s, which is acceptable for most applications.
3.4 DAC redundancy

Since we employed coarse comparators for several MSB decisions, DAC redundancy is necessary to tolerate potential errors made by the coarse comparators.

As shown in Figure. 29, in the binary search case, the search range is reduce by a factor of two in each cycle and each analog input can be mapped into one and only one digital code. Any time the comparator makes one wrong decision, it is determined to produce a wrong digital output code.

While in the case with redundancy [27], as shown in Figure. 30, the search range is reduced by a factor of less than two in each cycle and multiple digital codes can represent the same analog input. Errors made by the comparator within certain range can be tolerated by the redundancy.
Figure. 29. Binary search without redundancy

Figure. 30. Non-binary search with redundancy
Additional digital circuitry is needed to convert the raw output into N-bit digital code (in the case we showed here, the 4-bit raw output needs to be converted into 3-bit digital code).

Detailed implementation of the proposed SAR ADC is shown in the next chapter.
CHAPTER 4

In this chapter, we will discuss the different building blocks for SAR ADCs and their design techniques and considerations, such as capacitive DAC, sample and hold switch, comparators, SAR logics and calibration block. We will show some simulation results to justify the employed design techniques.

4.1 Capacitive Digital to Analog Converter (CDAC)

Figure 31. Set-and-down switching

The set-and-down [22] method is a power efficient switching scheme for SAR ADCs. As shown in Figure. 31. During sampling phase, the ADC samples the input signal on the top plates
of the capacitor bank and the bottom plates of the capacitors are connected to Vref. Next, the sampling switch opens and the capacitors are disconnected from the input. The comparator directly makes the first bit decision without switching any of the capacitors. According to the comparator output, one of the MSB capacitors is switched to ground while the other MSB capacitor remains at Vref. This process is repeated till the LSB decision. For each bit decision, the ADC only switches one capacitor, which reduces power consumption in both the capacitive bank and the DAC driving circuitry. The flow chart of the set-and-down switching method is shown in Figure. 32.

![Set-and-down switching flow chart](image)

Figure. 32. Set-and-down switching flow chart
However, large common mode jumps occur during charge redistribution, as shown in Figure 33. Since comparator speed, noise and offsets are all dependent on the input common mode, it is desired to have a constant common mode. The common-mode issue is addressed by splitting the capacitors [12], as shown in Figure 34. The waveform at the comparator input using the splitting capacitors for DAC is shown in Figure 35.

The weights of the 9-bit redundant codes are 128, 64, 32, 16, 10, 6, 4, 2, 1. During the four MSB bit decisions, a maximum error of 7 LSBs can be tolerated using this redundancy scheme, which is sufficient to cover both the settling errors and coarse comparator decision errors, according to simulations.
Figure 34. Capacitive DAC with constant common mode

Figure 35. Waveforms at comparator input with constant common mode
As shown in Figure 36, capacitors are built using custom-designed Metal-Oxide-Metal (MOM) capacitors with a unit capacitor of 0.3 fF using half finger capacitor [30]. The total capacitance seen at the summing node is 200 fF, where 80 fF is the switchable capacitance of the DAC, and 120 fF is the parasitic capacitance from the DAC, the comparators and the routings. The reference voltage needs to be scaled according to the ratio between the switchable capacitance and total capacitance.

Because of the small size of the unit capacitor that was used in our design, capacitor mismatch can potentially degrade the performance of the SAR ADC. As shown in Figure 37, the
capacitor mismatch mainly stems from the uncertainty of the edge of the metal lines, since the distance between the two metals is the critical parameter for the unit capacitor. The mismatch is ideally inversely proportional to the square root of the capacitor area [28]. However, the exaction tool does not take the edge uncertainty into account, so simulation of the capacitor mismatch is difficult.

![Figure 37. Cause of capacitor mismatch](image)

From the literature, [29] provides experimental data on capacitor mismatch characteristics, where a test structure and measurements results pertaining to the characterization of single-layer, lateral-field, 0.45-fF and 1.2-fF unit metal capacitors are presented. The measurement-inferred standard deviation for the capacitors are 1.2% and 0.8% respectively, as shown in Figure. 38.

Behavioral simulation of an 8-bit SAR ADC with 1.2% mismatch is shown in Figure. 39. In this behavioral simulation everything is assumes to be ideal except the capacitor mismatch. The
resulting 8-bit SAR ADC output spectrum shows an SFDR of 50.2 dB and an SNDR of 44.2 dB, which is sufficient for our design target.

Figure 38. Capacitor mismatch characteristics
In addition, various mismatch calibration algorithm can be applied to remove the effect of capacitor mismatch. Behavioral simulation of an 8-bit SAR ADC with 1.2% mismatch and foreground capacitor mismatch calibration is shown in Figure. 40. As we can see from the figure, the SFDR is improved to 54.9 dB and the SNDR is improved to 47.2 dB after foreground capacitor mismatch calibration.
Based on the foregoing study, we chose 0.6fF as a reasonable value for our unit cap, which provides enough input bandwidth and still maintain a good linearity. The detailed dimensions for the unit cap is provided in the table 1.
Figure 41: Unit capacitor

Table 1: Simulated comparator noise and power consumption

<table>
<thead>
<tr>
<th>Dimensions</th>
<th>Value (um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>G</td>
<td>0.65</td>
</tr>
<tr>
<td>H</td>
<td>6.0</td>
</tr>
<tr>
<td>S</td>
<td>0.13</td>
</tr>
<tr>
<td>W</td>
<td>0.13</td>
</tr>
</tbody>
</table>
4.3 Reference Buffer

Figure 42 shows why a reference buffer is needed. In conventional low speed SAR ADCs, people simply connect to the external voltage as reference voltage. However, this approach becomes problematic for the high-speed designs. The problem stems from the ringing on reference voltages caused by the inductance that is associated with the bonding wire. Even with pico Farads of bypass capacitors the ringing could still take up to a few nano seconds to settle, which is definitely unacceptable for our application, since our DAC needs to be settled with tens of pico seconds.

Figure 42. Ringing on reference voltage caused by bonding wire
Therefore, a low-power on-chip reference buffer is required in our design. A very power-efficient, low-output resistance clocked buffer in combination with MOS capacitor is described [12]. The reference voltage $V_{\text{ref}}$ used by the CDAC sets the gain of the ADC. It is controlled by an external voltage and buffered inside the ADC core. The target for the voltage buffer was a simple design at low power consumption. A capacitive recharging buffer, as shown in Figure. 43, is used. The external voltage $V_{\text{ext}}$ is compared with the internal reference voltage $V_{\text{ref}}$ using a clocked comparator. The clock $\text{ckres}$ is equal to the reset signal of the CDAC. Therefore the reference regeneration is initiated directly after the last decision. If $V_{\text{ref}}$ is smaller than $V_{\text{ext}}$, the output of the comparator triggers the attached inverter to add charge from $C_{\text{sw}}$ to the reference capacitor $C_{\text{ref}}$. The large $C_{\text{ref}}$ capacitor is implemented using MOS capacitors for maximum
capacitor density. By choosing the size of Csw, the percentage of recharging cycles is determined. To minimize noise on Vref, Csw should be chosen such that it is not too large but still provides sufficient robustness. This will result in a recharge of Cref most of the time.

A low output resistance of approximately 2 ohms is guaranteed by the large size of Cref. The main advantage of this buffer besides the low power consumption of 0.16mW are the guaranteed stability of the design and the low temperature dependence

![Simulation test bench of the reference buffer](image)

**Figure. 44.** Simulation test bench of the reference buffer

The simulation test bench of the reference buffer is shown in Figure. 44. The reference buffer is simulated with 1nH bonding wire inductance, 10pF bypass capacitor and 80pf reference capacitor. The simulated reference voltage variation is shown in Figure. 45.
Figure 45. Simulation results of the reference buffer

4.4 Sampling and Hold

Figure 46. Sample and hold switch
The schematic of the sample and hold switch is shown in Figure 46. CMOS switch is employed since the input common mode is about 500mV. The inline dummy switches are added in order to cancel the charge injection. The cross-couple dummy switches are added in order to cancel the signal feed through. Bootstrapped circuitry is not employed since our target resolution is 8-bit.

4.4 Comparator Design

Figure 47. Schematic of the comparator
Figure 48. Simulation results of comparator offset
The comparator employs a modified structure based on [31] as shown in Figure. 47. The first stage is essentially a charge domain pre-amplifier, which does not consume static current, followed by latch-type circuits as the second stage. Transistors M13 and M16 provide extra gain at the output of the pre-amplifier and reset the latch during the reset phase. M7 and M8 are used to reduce kickback noise. An extra input pair (M2 and M3) is used to calibrate the offset of the comparator.

Both the coarse and fine comparators use the same structure, but are sized differently. The power consumption of the coarse comparator is about one-fifth of that of the fine comparator, resulting approximately 35% comparator power savings.

When the clock signal is low, the comparator resets itself by charging the output of pre-amplifier to the supply voltage and discharging the latch output to ground. The reset switches should be sized such that a good and solid reset can be performed within the available reset time. Thus comparator is free of errors that caused by memory effect.

When the clock signal goes high, the comparator is activated and begins to make a decision based on the input. First, the output of the preamplifier is disconnected from the supply and the voltage at VMP and VMN begins to go down simultaneously but at a different rate based on the input difference. At some point, VMP and VMN becomes low enough and the latch stage take over, where the full digital level is regenerated.
Simulated comparator offsets of both the coarse and fine comparators are shown in Figure 48. Assuming Gaussian distribution, the offset $\sigma$ value is 7.3 mV and 15.6 mV for coarse and fine comparators, respectively. The calibration pair is sized accordingly to cover the $3\sigma$ range. All comparators are using the same structure, but sized differently to achieve different IRN. The reference comparator has the same size as the coarse comparator.

The input referred noise of the comparator is a crucial parameter. However, since the output of the comparator is digital ones and zeros, it is difficult to simulate or measure the comparator noise directly. On the other hand, we can simulate/measure the probability of ones and zeros at the comparator output. As shown in Figure 49, the output probability can be related to comparator input referred noise by the following equation.

$$P = \frac{1}{2} \left[ 1 + \text{erf} \left( \frac{V_{in}}{\sqrt{2V_n^2}} \right) \right]$$
Where $P$ is the output probability, $V_{in}$ is input voltage to the comparator and $V_n^2$ is the input referred noise of the comparator. Therefore, the input referred noise can be calculated once the output probability is known.

Figure 50. Comparator noise simulation
Figure 50 shows an example of comparator input referred noise simulation. The comparator is simulated at different input voltage. The probability of correct output at different input voltage is then curve-fitted to a normal distribution and the corresponding variance is the input referred noise voltage.

Table 2 Simulated comparator noise and power consumption

<table>
<thead>
<tr>
<th>Comparator Type</th>
<th>IRN</th>
<th>Energy/decision</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference comparator</td>
<td>1.98 mV</td>
<td>40 fJ</td>
</tr>
<tr>
<td>Coarse comparator</td>
<td>1.98 mV</td>
<td>40 fJ</td>
</tr>
<tr>
<td>Fine comparator</td>
<td>0.85 mV</td>
<td>196 fJ</td>
</tr>
</tbody>
</table>

4.5 Comparator Offset Calibration

The block diagram of the comparator calibration implementation is shown in Figure 51, where all five comparators’ outputs are fed into a pulse generation block and five sets of “up” and “down” pulses are generated, indicating whether the corresponding comparator has a positive offset or negative offset.
As discussed in section III, in order to reduce the effect of the noise on the offset control voltage, the up-down counter output code is updated every N cycle (N = 64 in our case). This is realized by adding accumulators in front of the up-down counters and clocking the up-down counter at a frequency of Fs/64, where Fs is the ADC sampling frequency. Finally, an 8-bit control DAC generates the control voltage “Vctrl” to control the calibration pair of the comparator.

Figure. 52 shows one of the pulse generation cells. The XOR gate detects whether the reference comparator and the comparator under calibration produce the same output bit. When the two output bits are different, only one of them will be set high. Depending on which bit is high, either “up” or “down” pulse is generated when there is a pulse at the enable signal “en”. The accumulators and up-down counters are synthesized using Verilog code.
One drawback of employing the control DAC and digital logics for calibration is the area overhead. Unit capacitor of 0.1fF is used for the 8-bit control DAC to minimize the area, since the linearity is quite relaxed for the control DAC. The total area for the offset calibration is approximately 25% of the total ADC area. Since the counter CLK and DAC refresh rate is 1/64 of the sampling clock, the power consumption of the digital logics is reasonably low (0.11 mW). The total power consumption of offset calibration is 0.34 mW, mainly consumed by the control signal generation, which operate up to gigahertz.

Figure 53 shows the simulation results of the comparator offset calibration. In simulation setup, transistor mismatch is enable so that different offset will show up in different comparators. The purple curve in Figure 53 is the offset control voltage for the reference comparator, and the other four curves are the offset control voltages for the four normal comparators.
As we can see from the figure, it took about 15 us for the offset control voltages to reach to steady states. The calibration converge time is acceptable to most applications.

Figure 53. Simulation of comparator offset calibration

Figure 54 shows the simulated ADC output spectrum before the offset calibration. As we can see from the figure, before offset calibration, the different offsets between different comparators caused large harmonic distortion in the ADC output spectrum, resulting an SFDR of 42.75 dB and an SNDR of 32.49 dB.
Figure 55 shows the simulated ADC output spectrum after the proposed offset calibration has converged. As we can see, the large harmonic distortions are removed in this case, resulting in an improved SFDR of 54.8 dB. The SFDR improvement is more than 10 dB comparing to the results shown in Figure 54. The SNDR also improved from 32.49 dB to 40.51 dB.
Figure 55. Simulated ADC output spectrum after offset calibration
4.6 SAR Logic

Figure. 56. SAR logic
The SAR logic implementation is shown in Figure 56. In each logic cell, signals “CMP_OUTP” and “CMP_OUTN” connect to the comparator output, “B_EN” enables the logic cell for specific bit, “To_DACP” and “To_DACN” are the control signals for the DAC, “To_MEMP” and “To_MEMN” deliver output bit stream into registers, and “start” and “finish” are used to trigger the bit cycling.

During the sampling phase, signal “start” is “0” and “finish_b” is “1” for all the logic cells, so the output of the NAND gate “B_ENB” is “1”. At the end of the sampling phase, “start” of the 1st bit logic cell switches to “1”, so “B_ENB” switches to “0”. This “1” to “0” transition will propagate to the comparator and triggers the 1st bit decision. When the comparators generate a valid digital output, signal “finish” becomes “1” and “finish_b” becomes “0”. The “finish” signal trigger the next bit cycling. “B_ENB” switches back to “1” because “finish_b” is “0” now. The same procedure happens for every bit and the corresponding pulse is generated for each bit. The desired comparator clocks are realized by simply combining corresponding pulses with NAND gates.

The intrinsic delay of the logic gates that forms the SAR logic provides a delay between the DAC settling and the rising edge of comparator clock. Simulations across different corners show that no extra delay element is necessary for the timing of DAC settling and comparator clock.

### 4.7 Digital Controlled Delay Line

A NAND based digital controlled delay line [32] is used to generate the sampling clock of the ADC. The duration of sampling clock can be controlled by the digital bits at the input of the
digital controlled delay line. The schematic of the digital controlled delay line is shown in Figure. 57.

Figure. 57. Digital controlled delay line

4.8 Simulation Results of the proposed SAR ADC

Figure. 58 shows the simulated output spectrum at low input frequency of the proposed SAR ADC. It achieves an SFDR of 53.99 dB and an SNDR of 42.67 dB, which equals to an ENOB of 6.8.

Figure. 59 shows the simulated output spectrum near Nyquist input frequency of the proposed SAR ADC. It achieves an SFDR of 52.35 dB and an SNDR of 42.13 dB. Since the input bandwidth is large enough, the performance degradation from low input frequency to Nyquist input frequency is almost negligible.
Figure 58. Simulated ADC output spectrum at low input frequency

Figure 60 shows the simulated SNDR of the proposed ADC at different process corners, which proves the robustness of the design. As expected, the SS corner results in the worst case performance. Since both the NMOS transistors and PMOS transistors are slower in the scenario of the SS corner case. Both comparator speed and SAR logic speed are compromised, which leads to the conversion speed degradation of the SAR ADC. For all 9 bit conversion to complete with one sample cycle, it requires about 1.1 ns in the SS corner case, which corresponding to a conversion rate of about 0.9 GS/s. As we can see from Figure 60, the ADC achieved an SNDR above 40 dB.
at 0.9 GS/s sampling rate in SS corner case. However, SNDR dropped below 40 dB when the sampling rate increase to 1GS/s. The SNDR degradation is cause by insufficient conversion time, which means the ADC does not have enough time to finish the last one or two conversion. In such cases, the supply voltage of the SAR ADC can be increased to compensate this speed degradation cause by slow transistor speed. Because with a higher supply voltage can increase the speed of both comparators and SAR logics.

Figure 59. Simulated ADC output spectrum near Nyquist input frequency
For TT corner, the proposed SAR ADCs maintains an SNDR above 40 dB up to 1GS/s and even at 1.1GS/s, it still achieves an SNDR of about 37dB.

For FF corner, the proposed SAR ADCs can achieve close to 40 dB SDNR all the way up to 1.2 GS/s

Figure. 61 shows the simulated SNDR performance versus input frequency. As we can see from the figure, the SNDR is quite flat up to Nyquist input frequency.
Figure 61. ADC simulation results at different process corner
CHAPTER 5

5.1 ADC Measurement Setup

The block diagram of the ADC measurement setup is shown in Figure 62. Since we perform a single tone sine wave test to characterize the performance of our ADC, the signal generator first generates a sine wave signal. The sine wave input signal is then fed into a low-pass filter to filter out the high frequency noise. After that, it goes through a balun, so that the single-end signal is...
converted into a fully differential signal. Since the input common mode is controlled by a separate DC source. The input signal goes through a DC block before it is fed into the chip.

Another signal generator is used to provide the clock signal to the chip, which also goes through a filter and balun before it is fed into the chip. An external current source is used to bias the on-chip clock buffer, which converts the differential clock into a single-end CMOS clock.

A DC source is employed to provide ground, supply and input common mode voltage to the chip.

Digital control bits are sent into the chip by an SPI interface and the final digital output data is sent to the digital core and saved in the on-chip memory. The output data is later read out into PC at a much slower speed and post-processed in the Matlab.

All pads of the chip are wire-bonded to the package except the input pad are probed. The packaged chip sits on a motherboard that includes a Micro Controller Unit (MCU), which enables communication to PC. For measurement cost reasons, a “discrete” probing system is used instead of a commonly used probe station. The discrete probing system includes an anti-vibration table, an X-Y positioner, probes and a digital microscope. Figure 63 shows the photo of the probe testing setup.
Figure 63. Probe testing
5.2 Measurement Results

The prototype ADC was fabricated in a 28 nm CMOS process with a core area of 150 \( \mu \text{m} \times 45 \mu \text{m} \). The die photo and the corresponding layout is shown in Figure. 64.

The input signal was feed into the chip via RF probes, while clock and DC signal were wire-bonded. The output data was captured by the on-chip SRAM and then read out to a PC through an
Figure. 65. ADC output spectrum, comparator offset calibration off

Figure. 66. ADC output spectrum, comparator offset calibration on
SPI interface. Capacitor mismatch was calibrated in foreground. The ADC operates with a nominal differential input swing of 550 mVpp at a nominal supply voltage of 0.9 V. Figure 65 and Figure 66 capture the ADC output spectrums at 1 GS/s sampling rate with near Nyquist input frequency for scenarios of with and without comparator offset calibration.

Figure 67 shows the SNDR and SFDR of the ADC output spectrum with different input frequencies at a sampling rate of 1 GS/s. The measured SNDR is almost flat with input frequency, achieving 43.6 dB near Nyquist frequency. Figure 68 shows the SNDR of the ADC output spectrum at different sampling frequencies with different supply voltages. Higher supply voltage
increases the maximum sampling rate because both comparator and SAR logic operating faster with a higher supply voltage but at the cost of higher power consumption.

Figure 68. SNDR versus sampling frequency

Figure 69 gives the power breakdown based on simulation results: 0.98 mW for fine comparators, 0.18 mW for coarse comparators, 1.22 mW for SAR logic, 0.36 mW for DAC, 0.16 mW for the reference buffer, and 0.34 mW for the comparator offset calibration. The total power consumption at 1 GS/s is 3.2 mW. Figure 70 plots the ADC gain vs input frequency. The
3-dB input bandwidth is about 4 GHz. Figure 71 gives the measured DNL and INL of ADC, which are both within ±0.5 LSB.

Figure 69. Power breakdown
Figure 70. Gain versus input frequency

Figure 71. DNL & INL
The comparison to previously reported work is shown in Table II. Calculated FoM of the ADC is 21.82 fJ/conv at 0.85 V supply, 25.87 fJ/conv at 0.9 V and 31.93 fJ/conv at 0.95 V. At 1.3 GS/s, the ADC still achieves an SNDR of 33.2 dB and an ENOB of 5.2. The core SAR ADC area is 0.00235 mm2, the reference capacitor area is 0.0027 mm2 and offset calibration logic area is 0.0017 mm2, resulting a total area of 0.00675 mm2. To the best of our knowledge, this ADC achieves the highest SNDR among all single-channel SAR ADCs reported to date operating above 1 GS/s, with a very competitive FOM.

Table 3  Performance Comparison.

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CHAPTER 6

6.1 Conclusion

A novel SAR architecture capable of operating at 1 GS/s with 3.2 mW achieving an SNDR of 43.6 dB is presented. Coarse and fine comparators are employed in this design to minimize the power consumption. A design methodology is proposed for optimizing the configuration of coarse/fine comparators. Offsets between different comparators are calibrated in fully background mode using the proposed reference comparator calibration scheme, which removes the calibration time from the SAR timing budget completely.

6.2 Future Work

Besides interleaving multiple channels of SAR ADCs together to achieved higher aggregate sampling rate. A hybrid structure as a pipelined SAR has the potential to further increase the speed of a single channel SAR ADC. For low power purposes, the high-power close-loop residue amplifier can be replace by a open-loop residue amplifier and the gain variable can be calibration digitally.
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