Fall 2018

Using GS/s ADC to Evaluate the EMI of GaN-based Power Devices

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USING GS/S ADC TO EVALUATE

THE EMI OF GAN-BASED

POWER DEVICES

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A Thesis Presented to the Graduate Faculty of

Lyle School of Engineering

Southern Methodist University

in

Partial Fulfillment of the Requirements

for the degree of

Master of Science in Electrical Engineering

with a

Major in Electrical Engineering

by

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December 15, 2018

ACKNOWLEDGMENTS

I would like to convey my greatest appreciation and gratitude to the advisor of my graduate project, Prof. Ping Gui. The entire project was completed under her guidance. She is not only highly professional and knowledgeable in related fields, but also greatly kind to her students.

Meanwhile, I must express my appreciation to the other two committee members of my graduate project, Prof. Jennifer Dworak and Prof. Theodore Manikas, who support me in revising and improving the project.

Most importantly, I have to show the most gratitude to my parents for their support to my academic career.

Zhang, Chi B.S., Information Engineering, Beijing Institute of Technology, Beijing, 2016

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Advisor: Professor Ping Gui

Master of Science conferred December 15, 2018

Thesis completed November 2, 2018

As the silicon-based power devices are gradually reaching their performance limits, new power transistors such as Silicon Carbide (SiC) and Gallium Nitride (GaN) FETs have been rapidly developed in recent years. GaN devices have been widely accepted by researchers for its higher speed and efficiency than silicon power devices. However, despite all its merits, the GaN device faces a more severe problem of electromagnetic interference (EMI) than the silicon device due to its high performance. Various control techniques of EMI have been studied so far and many of them require the evaluation of EMI. Research shows that the EMI level of switching converters is related to the switching node voltage. Therefore, sensing the switching node could provide a possible solution for the EMI control.

In this thesis, an EMI evaluation method is proposed. The approach is to evaluate the EMI by sensing the switching node voltage with a giga-sample per second (GS/s) analog-to-digital converter (ADC). In order to verify the feasibility of the proposed method, a synchronous DC-DC step down (buck) converter is built. Measurements are carried out

in both time and frequency domain. Experimental results proved this evaluation idea is a possible solution for the EMI evaluation.

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CHAPTER 1
INTRODUCTION

1.1 Background

Approximately 40 years ago, one of the earliest commercially viable silicon MOSFETs was introduced by International Rectifier, to take the place of bipolar devices in switch mode power supplies (SMPS) [1]. Since then, this silicon-based power device has been thoroughly developed to fit in all sorts of working conditions. However, silicon-based technology is reaching its performance limit, where the further development is becoming cost prohibitive. In order to stretch the limit, researchers have studied different semiconductor materials to take the place of the silicon device. In the field of power electronics, wide bandgap materials, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), shows the most potential to meet the requirement of next generation applications.

The first GaN based High Electron Mobility Transistor (HEMT) was a depletion mode RF transistor made by Eudyna Corporation in Japan in 2004 [2] with its own merits. Comparing to a conventional silicon power device, it can operate at much higher frequency with larger power density. Also, the transistor could resist high voltage because of its high electron mobility. SiC based devices also have the comparable performance of GaN based devices but GaN is better because of its lower price.

In spite of these advantages, the employment of GaN FETs also brings a significant drawback: electromagnetic interference (EMI). EMI in power electronic applications is

unavoidable because of the discontinuity of current. Research shows that the high slew rate (di/dt) of current and voltage (dv/dt) would cause ringing and overshooting in signal [3]. Thus, the higher performance of the GaN device leads to a more severe EMI problem. As a result, additional care needs to be taken in the GaN device's driver circuit.

Traditionally, designers use filters to mitigate the EMI effects at the source of the switching power converters [4] or they just decrease the driving current to ensure a low slew rate. However, using these methods in SMPS systems either requires extra space for installation or decreases the efficiency. Moreover, while designing the filter, designers face the challenge of estimating the EMI level with reasonable accuracy for different structure and operating conditions. Smart drivers that can supply current based on the EMI level of GaN FETs are introduced to increase the efficiency and stability [5]. They also need to evaluate the EMI level of the system in order change the driving strength. Hence, the evaluation of EMI in GaN-based SMPS is always critical.

In this paper, I utilize a GS/s high-speed successive approximation register (SAR) ADC to sense the switching node voltage in order to evaluate the EMI level of a DC-DC step-down converter (buck converter). According to [6], EMI is related to the voltage level of the switching node. This evaluation approach has a great advantage that it is easier to analyze the signal in both the time domain and frequency domain, which can give the driver designers a better idea of the EMI level.

1.2 Objectives

The aim of this thesis is to verify the feasibility of the proposed EMI evaluation approach, using a GS/s ADC to sense the switching node voltage of a power converter. The text focuses on the following objectives:

- A detailed study on the high speed GaN-based power devices and the EMI issues of switching power converters. This includes the control method of GaN FET drivers.
- Construction of a DC-DC step-down (buck) converter with an existing GaN FET evaluation board.
- Measurement of the buck converter's switching node voltage with a GS/s ADC and a comparison of the result with the correct value in order to evaluate the EMI level.

1.3 Outline

This paper is organized in the following way:

- Chapter 2 introduces the background of the research. The GaN FET basics, EMI of the converters and the SAR ADC are discussed with detailed information.
- Chapter 3 illustrates the system thoroughly with schematics and PCB design. Simulation results are also presented in this chapter.
- Chapter 4 contains the switching node voltage measurement procedure as well as the testing results from ADC.
- Chapter 5 concludes the overall testing result and states the future development for this project.

CHAPTER 2
BACKGROUND

2.1 GaN HEMT Basics

2.1.1 Development of Power semiconductor

The development of power semiconductor began around the 1950s when silicon devices took the place of germanium and selenium devices [7]. Since then, silicon transistors in power electronics has evolved rapidly. In the 1960s, the first silicon based bipolar transistor with the capability of handling the power electronics applications was introduced. Then, with the advancement of semiconductor industry, silicon power MOSFETs became available in the 1970s as alternatives to bipolar transistors [8]. To combine the advantages of both power bipolar device and MOSFETs, the Insulated Gate Bipolar Transistor (IGBT) was fabricated in the early 1980s [9].

Although silicon-based power devices have been dominated the market since the mid-1990s for its reliability and affordability, they have now reached a theoretical limit because of the material's physical properties. Plenty of efforts have been made by the researchers trying to overcome this problem but most of the solutions came with substantial cost. As a result, the power industry must now move on to new semiconductor materials to meet the requirements of the emerging applications. Wide bandgap semiconductor materials have been studied widely in the recent years as the next generation material, among which Gallium nitride (GaN) has shown great promise in the high speed and high voltage designs.

2.1.2 Characteristics of GaN HEMT

Table 2.1 and Figure 2.1 both show the properties of silicon and wide bandgap materials (SiC, GaN). The bandgap energy is related to the amount of energy it takes to break the chemical bonds inside the crystal. The harder it is to break the bonds inside the material, the harder it is to pull out electrons. SiC and GaN have a bandgap energy about three times that of silicon, so they are called wide bandgap semiconductors. These wide bandgap materials have a higher critical breakdown electric field. In the case of GaN, 3.3MV/cm means that if two terminals in a GaN device is 1cm apart from each other, they could withstand 3,300,000V before getting an avalanche. GaN and SiC's breakdown electric field is about an order of magnitude higher than silicon. As a result, two electrical terminals in a GaN or SiC device can be 10 times closer than that in silicon device to block the same amount of voltage.

The higher mobility of GaN and SiC can reduce the ON-resistance (R_{ON}) of the transistor, which makes it possible for a smaller size device to obtain the same amount of current. Higher saturation speed and lower R_{ON} lead to an improvement on efficiency.

Although SiC outperforms GaN in high-temperature conditions due to its higher thermal conductivity, it suffers from excessively high cost. [12] As a result, among all the new semiconductor materials, GaN based device is outstanding in high-efficiency, high-frequency and high-voltage power applications.

Table 2.1 Material properties of GaN, SiC, and silicon [10]

Material Property	Si	SiC-4H	GaN
Band Gap (eV)	1.1	3.26	3.39
Critical Breakdown Electric Field (MV/cm)	0.3	3.0	3.3
Electron Mobility (cm^2 /V-sec)	1350	700	2000(2DEG)
Electron Saturation Velocity (10^7cm/sec)	1.0	2.0	2.5
Thermal Conductivity (Watts/cm K)	1.5	4.9	1.3

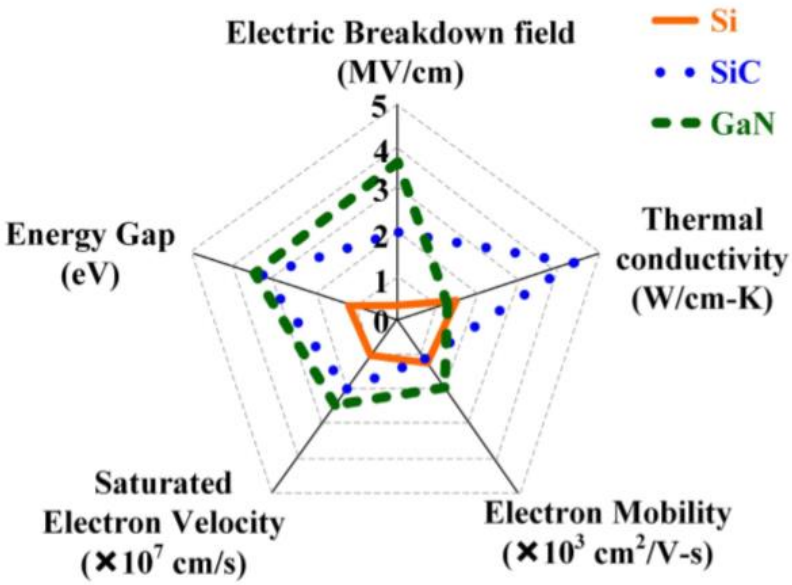


Figure 2.1 Comparison of Si, SiC, and GaN for power semiconductor applications [11]

2.1.3 Basic GaN HEMT Structure

The operation of GaN HEMTs is similar to that of silicon power MOSFETs but their structure is significantly different. GaN is naturally piezoelectric material [13]. This means that when a crystal is strained, it will produce a small voltage. If a very thin layer of AlGaN is added to the surface of GaN, a lot of strain can be created over a very small distance. This builds up an electric field that attracts electrons to the interface creating the two-dimensional electron gas (2DEG). This conductive 2DEG have the similar function as the "channel" in silicon MOSFETs. It can be used to conduct large amount of current, as shown in Figure 2.2. The 2DEG can be turned off by applying a positive voltage from the GaN layer to the AlGaN layer which attracts away the electrons in the 2DEG.

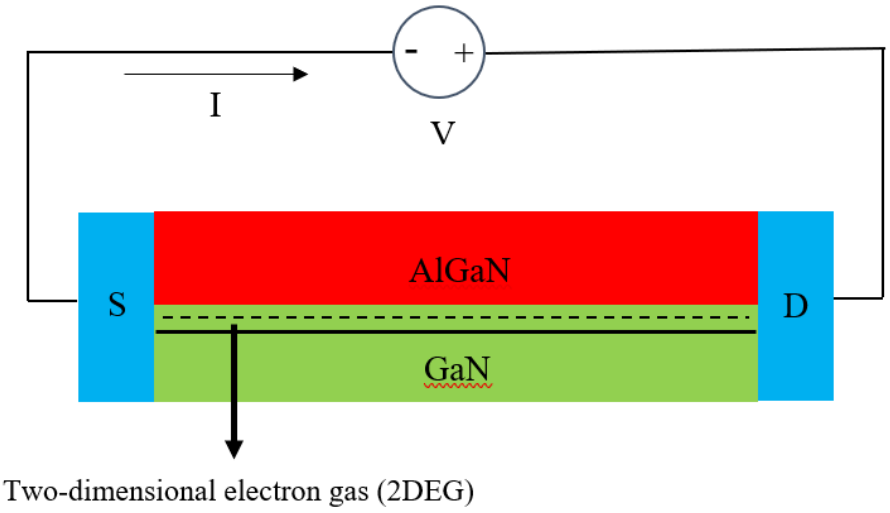


Figure 2.2 Two-dimensional electron gas (2DEG) in GaN device

The basic GaN transistor structure is based on the simple structure in Figure 2.2. An important property of GaN is that it could be grown on a thin layer on top of silicon, which greatly decreases the price of the GaN HEMTs because the silicon is much more

inexpensive than GaN [14]. As depicted in Figure 2.3, the GaN layer sits on top of the silicon substrate (GaN-on-silicon structure). The AlGaN layer introduces strain to the GaN and forms the 2DEG. Same as silicon transistors, GaN transistors also have gate, source, and drain node. This type of GaN HEMT serves as a normally on transistor because the 2DEG always exists when there is no voltage on the gate node. In order to deplete the 2DEG, a negative voltage needs to be applied to the gate, and then the transistor could be turned off. This type of transistor is called a depletion mode, or d-mode transistor.

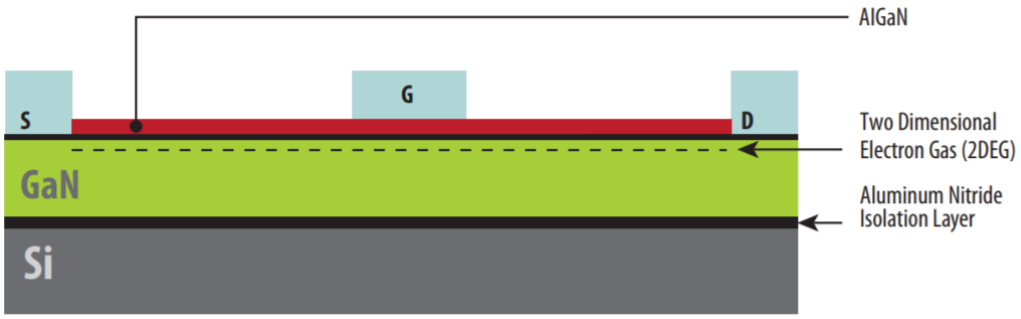


Figure 2.3 Typical GaN FET structure with three metal-semiconductor contacts for the source, gate and drain. [15]

2.1.4 eGaN HEMT Structure - Enhancement Mode

Depletion mode devices are not desirable in power electronics because they require a negative voltage at the gate to turn the device off. If a negative voltage is not first applied to the gate, the device acts like a short circuit, which may cause a hazard. To build a

normally off device by depletion mode transistors, the cascode structure in Figure 2.4 can be implemented.

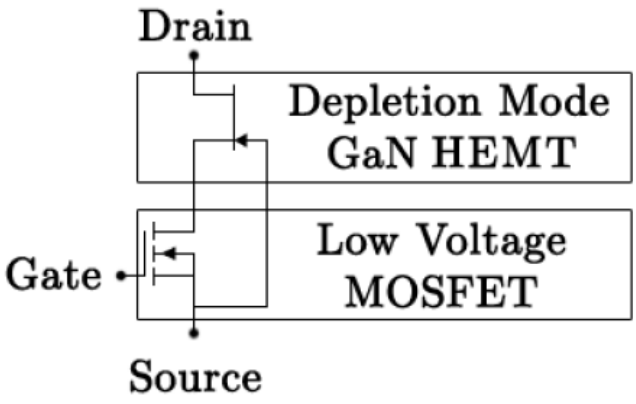


Figure 2.4 Cascode GaN device [16]

Normally off GaN device without cascode structure is also available recently. For example, Efficient power conversion (EPC) has developed a proprietary technology for making a gate electrode which is able to pull away the electrons with zero volts on the gate, as seen in Figure 2.5 [15]. A positive voltage is needed to form the 2DGE on the surface of the GaN layer. This type of device is called an enhancement mode device.

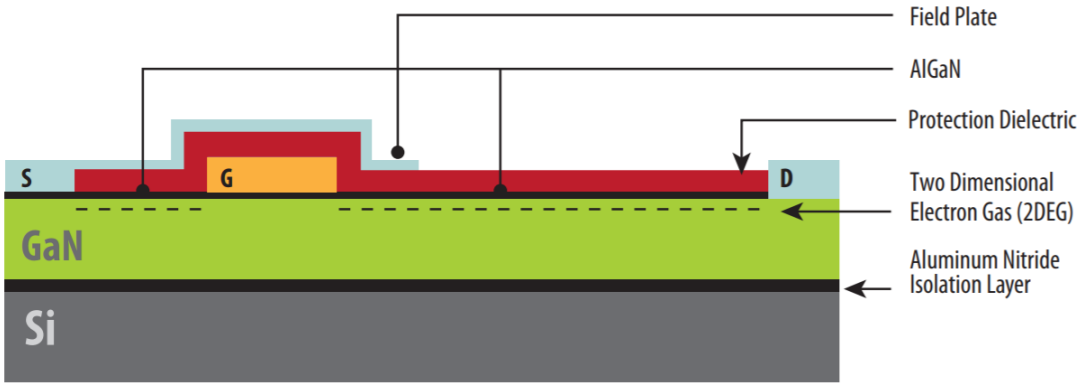


Figure 2.5 eGaN HEMT structure [15]

In this thesis, the GaN HEMTs we used are enhancement mode transistors.

2.2 Buck Converter

2.2.1 Basic Configuration

The most basic switch mode switch mode power supplies (SMPS) are buck (DC-DC step down) and boost (DC- DC step up) converters. These power converters have two topologies: non-isolated and isolated. Non-isolated means the input and output voltages share a common ground. The isolated topology has the opposite definition. Each topology has its unique properties. In this thesis, a non-isolated buck converter is built for the EMI evaluation.

A buck converter is desired when the output of the power supply needs to be lower than the input. Comparing to the linear regulator, a circuit with the similar function of buck converter, the buck converter has a much better power efficiency. A typical buck circuit with a power MOSFET driver is shown in Figure 2.6. There is an n-type MOSFET (M1) serves as a switch, controlled by the driver circuit which provide a Pulse Width Modulation (PWM) signal to the transistor. The diode (D1) is usually called the catch diode, or freewheeling diode. [17] The inductor (L1) and capacitor (C1) form a LC filter for the output. The parasitic components are not drawn in the picture, but they will have a great influence to the EMI of the system. The resistor (R1) on the very right stands for a load of the power stage. A constant output voltage can be produced at V_{OUT} with a constant input and the step-down ratio is determined by the driver circuit. This type of buck converter is called asynchronous buck converter.

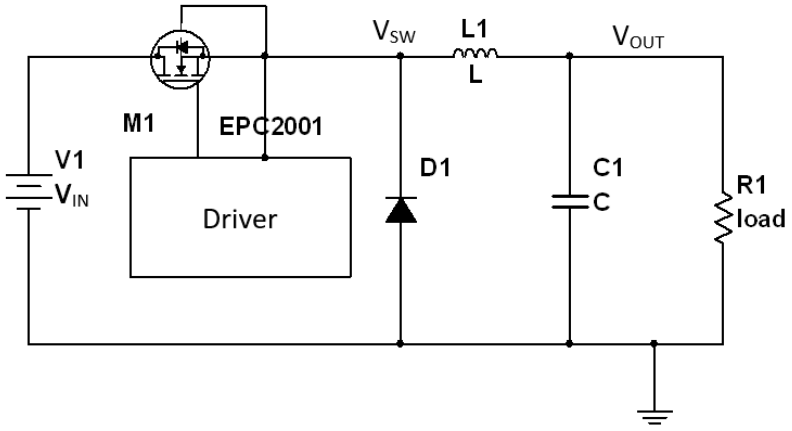


Figure 2.6 Asynchronous buck schematic

If the diode is replaced by another power MOSFET as seen in Figure 2.7, this buck converter is called a synchronous buck converter, because M2 switches on and off synchronously with the M1.

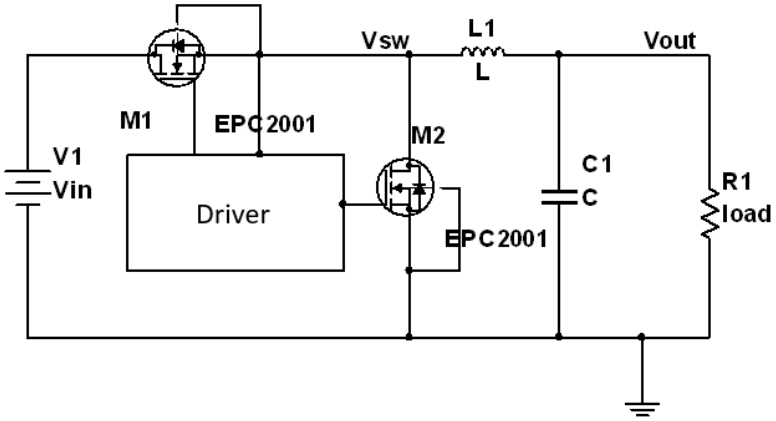


Figure 2.7 Synchronous buck schematic

Comparing to the asynchronous topology, the synchronous buck converter has a much less power loss with the low on-resistance of the low side transistor (M2) [18]. Nevertheless, it requires a more complicated driver to control the two power devices.

Dead time control is needed to prevent the high side switch (M1) and the low side switch from turning on at the same time.

2.2.2 Operation of Buck Converter

There are two operating modes for the buck converter: continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

In both modes, the operation of the buck converter can be divided into two states in every switching cycle: The ON state is when M1 is ON and the M2 is OFF. The OFF state is the opposite condition. The simplified circuit for both states is drawn in Figure 2.8, where the transistors are replaced by their equivalent components.

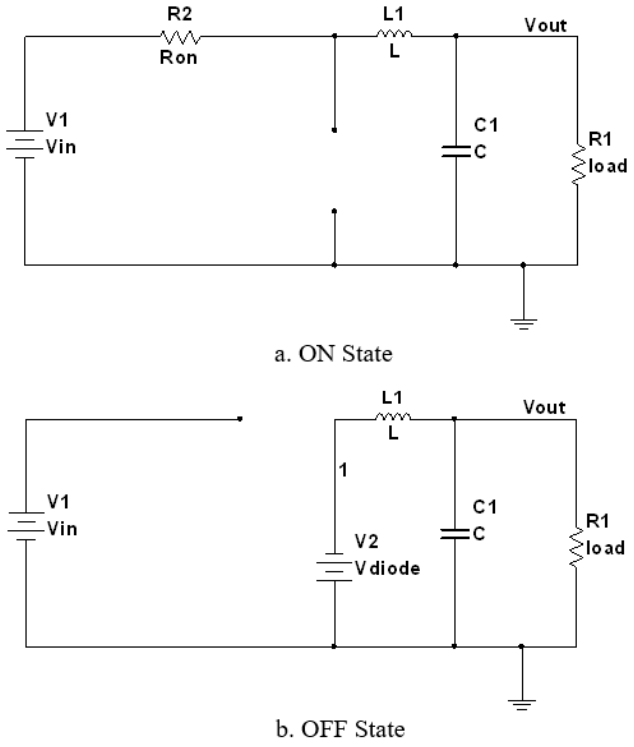


Figure 2.8 Buck operating states

The time interval of the ON state is $D \times T_S = T_{ON}$, where D is the duty cycle, set by the control circuit (typically a PWM signal generator), defined as a ratio of the transistor M1's time of switched on to the time of one complete period, Ts. T_{OFF} represents the duration of the OFF state. Since there are only two states per switching cycle for continuous mode, T_{OFF} is equal to $(1 - D) \times T_S$. The quantity $(1 - D)$ is sometimes called D'. These time intervals for CCM are shown along with the waveforms in Figure 2.9 [19].

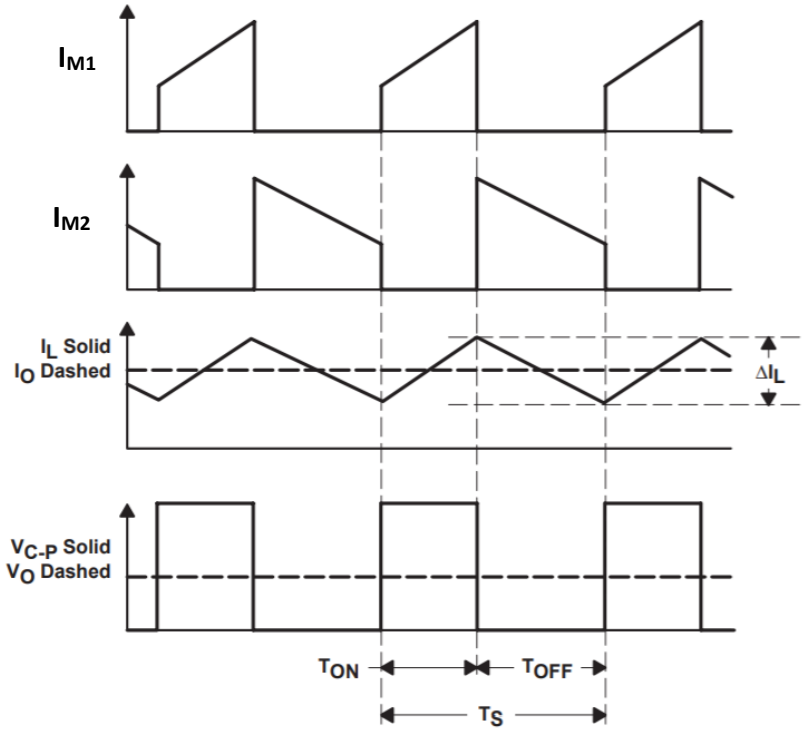


Figure 2.9 Continuous-mode buck power stage waveforms [19]

As shown in Figure 2.8 and 2.9, in continuous current mode, the current passing through the inductor is always above 0A, which represents "continuous current". In this operating mode, the current through the inductor only flows in one direction.

Assuming the average current flowing through the inductor is constant, it is easy to find out the relation between input voltage and output voltage:

$$\frac{Vin - Vcp}{L} \times DTon = \frac{Vcp}{L} \times (1 - D)Ton$$

Therefore,

$$\mathrm{D} = \frac{Vcp}{Vin}$$

where Vcp represents the average output voltage.

This equation means the output voltage is only dependent on the duty ratio of the PWM signal and the input voltage.

For DCM, the current passing the inductor can reduce to 0 while in OFF state, as shown in Figure 2.10. This results in a much more complicated calculation. In this thesis, the buck converter is designed to work in CCM mode.

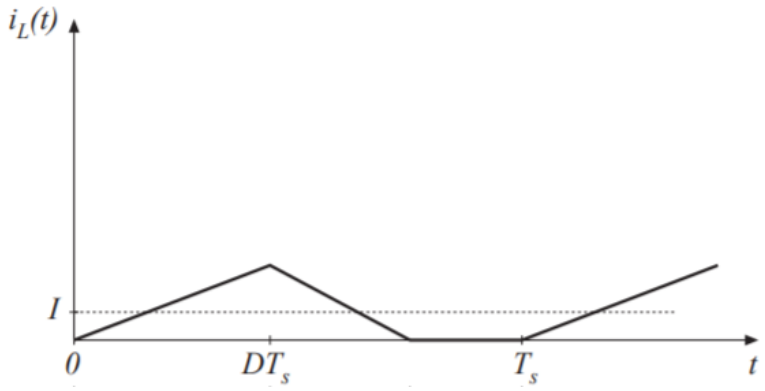


Figure 2.10 DCM current waveform [19]

2.3 EMI of Switch Mode Converters

2.3.1 EMI Basics

Switch mode converters always come up with electromagnetic interference (EMI) problems due to their nature of fast switching voltages (dv/dt) and currents (di/dt). The rapid changing in current or voltage causes more high-frequency components in their output spectrum.

The most obvious observation of the EMI is measuring the switching node voltage (Vsw). A Vsw with EMI issue is shown in Figure 2.11. Instead of a clean pulse wave, the waveform in the picture has significant overshooting and ringing. The maximum overshooting value and the ringing frequency is related to the EMI level of the converter [6].

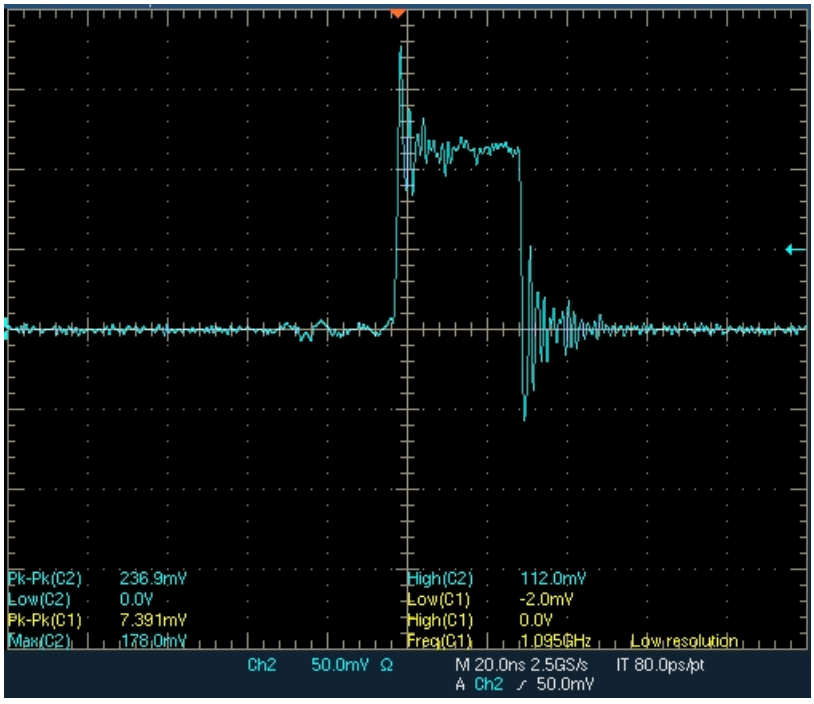


Figure 2.11 Observation of the Vsw with EMI presented

The synchronous buck converter typically generates three types of EMI: low frequency conducted noise (<30 MHz) as harmonics of the switching frequency, broadband noise (50 – 300 MHz) from the phase voltage ringing, and high frequency noise (>300 MHz) as a result of reverse recovery [20].

Figure 2.7 shows the ideal circuit of buck switching converter, while in an actual circuit, there will always be a lot of stray capacitors and inductors as shown in Figure 2.12. When the high-side transistor is turned on, the energy that is stored in the parasitic components will lead to resonance in the input loop. This switching loop can be modeled as an RLC circuit [22]. It is built up of the input capacitor and both high side and low side transistors. Very small values of stray components could cause resonance frequencies over several hundred MHz on the switching node. Therefore, evaluation of the EMI level of power converters can be realized by monitoring the switching node voltage.

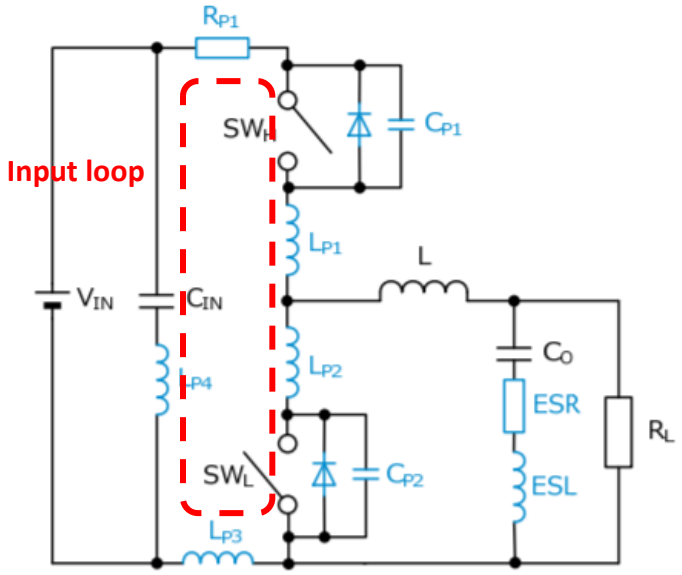


Figure 2.12 Buck converter with parasitic components [21]

2.3.2 EMC Standard

Electromagnetic compatibility (EMC) is the ability of electronic and electrical systems or components to work properly when they are close together [23]. This indicates that electronic and electrical equipment should have the ability to lower the noise they generate so that they won't disturb others. Also, they ought to be immune to the interference in the environment. That is saying, electrical devices need protection against electromagnetic interference (EMI) to guarantee the system's performance. Meanwhile, they should not interfere with other devices. Before the electronic devices enter the market, many nations and standards require all the electronic products to satisfy the EMC standards.

To regulate the allowable levels of conducted and radiated emissions generated by a product, a large amount of Electromagnetic compatibility (EMC) standards have been introduced, such as CISPR (Commitee International Special des Perturbations Radio) standard, FCC (Federal Communications Commission) standard, ANSI (American National Standards Institute) standard, IEC (International Electrotechnical Commission) standard, etc. [24]. The EMC standard which people choose to comply with is based on the application area of the electronic products. Different standards have different requirements for the test setups, measurement equipment, measuring bandwidth, noise limits and so on.

As an example, Figure 2.13 depicts the CISPR 25 EMI emission standard. It sets a limit for the magnitude of the signal's spectrum.

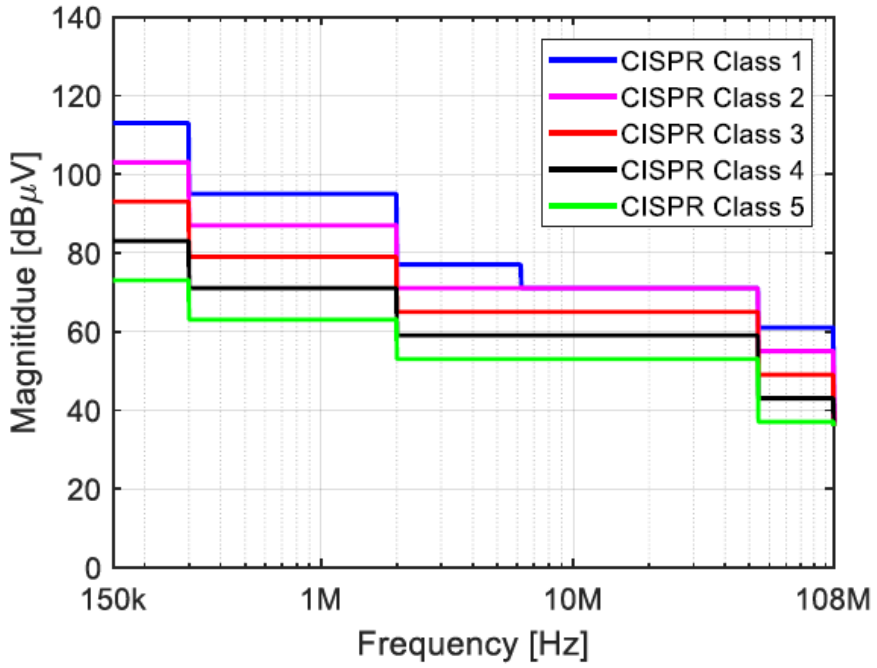


Figure 2.13 CISPR 25 EM emission standard [24]

2.4 GaN FET Driver Controlling

In order to reduce the EMI in switch mode converters, a common approach is to apply EMI-filters at the input of the converter [25]. However, these filters are bulky and cannot be integrated on the chip of the power switch. What's more, in some situations, the EMI filters play as a role of undesired additional parts on the circuit board as they may cause extra costs, space and weight. Consequently, the generation of EMI has to be prevented by other methods. One of the solutions is the active gate current control strategy implemented on the GaN FET drivers, as discussed in [26] and [27].

Most of the control techniques require voltage or current sensing to provide the reference for the driver to change its driving strength. Some designers use an oscilloscope to monitor the EMI level directly [28]. In this thesis, an ADC-based sensing method is verified to aid the GaN HEMTs active driving in the future.

2.5 ADC Used in Voltage Sensing

2.5.1 SAR ADC

Successive-approximation-register (SAR) analog-to-digital converters (ADCs) are usually the choice of medium-resolution and high-resolution applications because of their low power consumption and simple structure.

The basic architecture of SAR ADC is presented in Figure 2.14. A track and hold (T&H) circuit samples the analog input (Vin) and hold the value for the conversion. To perform the binary search algorithm, the ADC starts by setting the N-bit register to half of the reference voltage (V_{REF}), which means setting the MSB to 1 and other bits to 0. Then the comparator will compare the value of the sampled Vin and the reference voltage. If Vin is larger than V_{REF}, the output of the comparator will be a logic high (1) and the MSB of the register will remain at 1. On the other hand, if Vin is less than V_{REF}, the comparator output will be 0 and the MSB of the register will also be reset to 0. This is the end of the first conversion. The DAC generates the reference voltage ($V_{REF}/2$) for the next conversion. The ADC will repeat this procedure for N times (N is the resolution) until it achieves the LSB. Once it has the LSB, the conversion is complete and the N-bit digital output will be available in the register. As illustrated above, the SAR topology can finish all the conversion with only one comparator, which significantly simplifies the ADC structure.

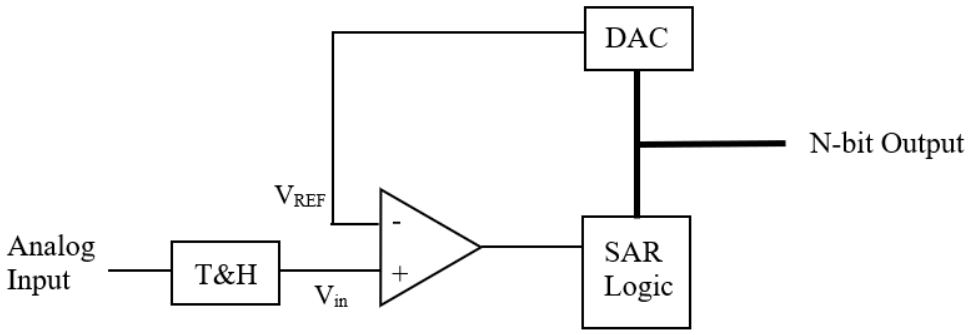


Figure 2.14 Basic SAR structure.

Figure 2.15 shows an example of the SAR binary search operation (4-bit conversion). The y-axis represents the reference voltage produced by the DAC. As in the picture, the first comparison shows that Vin is less than V_{REF}. Therefore, the MSB is set to 0. The reference is then set to 0100 and this time, Vin is greater than the reference so the second bit remains at 1. In the third conversion, V_{REF} is set to 0110 and the comparison sets the third bit to 0. In the last comparison, input voltage is larger than the V_{REF} so the LSB is set to 1 and the final output is 0101.

The operating scheme of the SAR ADC makes it hard to achieve both high speed and high resolution at the same time because it has to compare the input and the reference for each single bit. However, it's low power and space consumption make the SAR topology outstanding to be integrated with other larger functions.

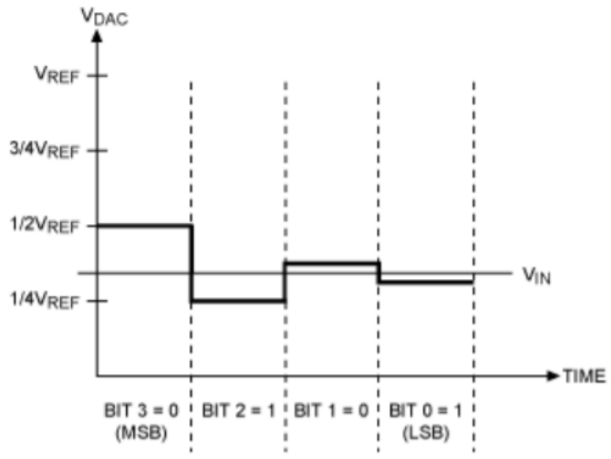


Figure 2.15 SAR operation.

An ADC with SAR topology is selected in this thesis for high accuracy as well as low power consumption in the measurement.

2.5.2 The ADC implemented in this thesis design

A recent work on a 1GS/s 8-bit SAR ADC has demonstrated that it can operate at 1GS/s with 8-bits with a power consumption of around only 3mW and it has the highest SNDR (43.6dB) among all single channel SAR ADC reported that operates above 1GS/s when it is published (2017) [29].

The architecture of this SAR ADC is shown in Figure 2.16. Modifications have been made on the comparators. Comparators with different input referred noise (the coarse and the fine comparators) are employed in order to perform bit decision efficiently. The calibration time is removed from the timing budget for the implementation of the reference comparator, which makes it possible for higher speed conversion.

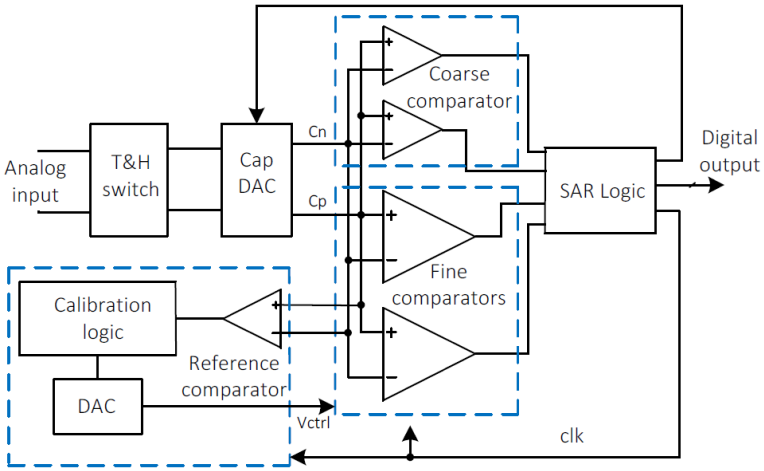


Figure 2.16 Block diagram of the ADC. [29]

CHAPTER 3
SWITCHING NODE VOLTAGE SENSING

This chapter discusses the ADC-based switching node voltage (V_{SW}) sensing scheme. Simulation results are also presented in this chapter.

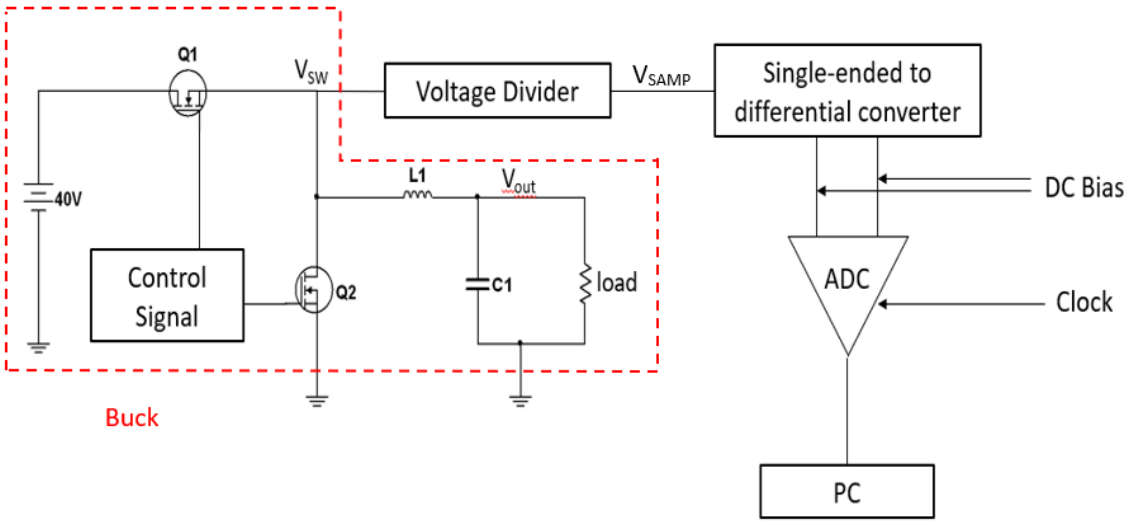


Figure 3.1 Schematic of the design

Figure 3.1 shows the overall schematic of the design. As indicated in the Chapter 2, a DC-DC step down (buck) converter is built to produce the switching node voltage (V_{SW}) for the ADC to measure. The voltage divider consists of two sampling resistors, which can scale down the switching node voltage to the input range of the ADC. The scaled down voltage V_{SAMP} is converted into differential outputs by a single-ended to differential converter for high speed signal transfer. Next, the ADC samples the V_{SAMP} and stores the result in the memory on the ADC chip. Then, it feeds the digital data to a computer to process in digital domain. Both time domain information and the spectrum of V_{SW} are produced by the computer.

In this and the following chapters, the measurement of V_{SW} will be implemented on a synchronous buck converter which transforms a 40V DC voltage to a 1.2V DC voltage at 1MHz.

3.1 GaN Device Selection

EPC8002 GaN FET is chosen as the switching transistor in this design for it has a relatively small figure of merit ($Q_g \times R_{ON}$). Figure of merit is a generally accepted performance and efficiency indicator for power MOSFETs [30].

To minimize the influence to the final sensing result from the buck circuit, we use a pre-produced evaluation board of EPC8002 to build the converter. As shown in Figure 3.2, it already has the optimized set-up for a buck converter without the output stage (the external circuit in Figure 3.3), which can provide a valid switching node voltage for the ADC to measure later. An interface board with the output stage of the buck is stated in the next section.

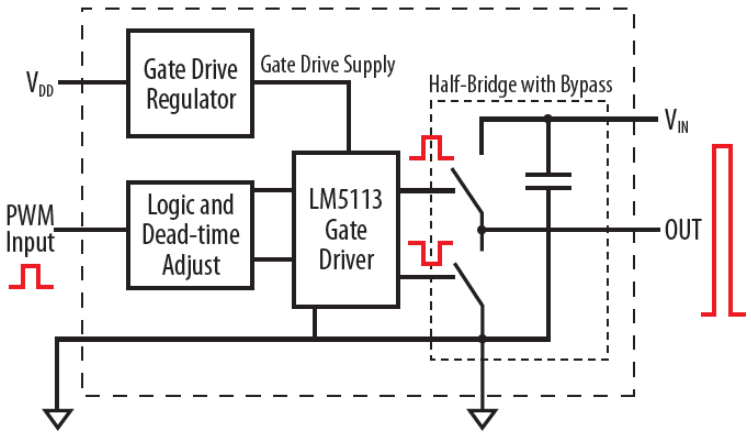


Figure 3.2 Block diagram of evaluation board [31]

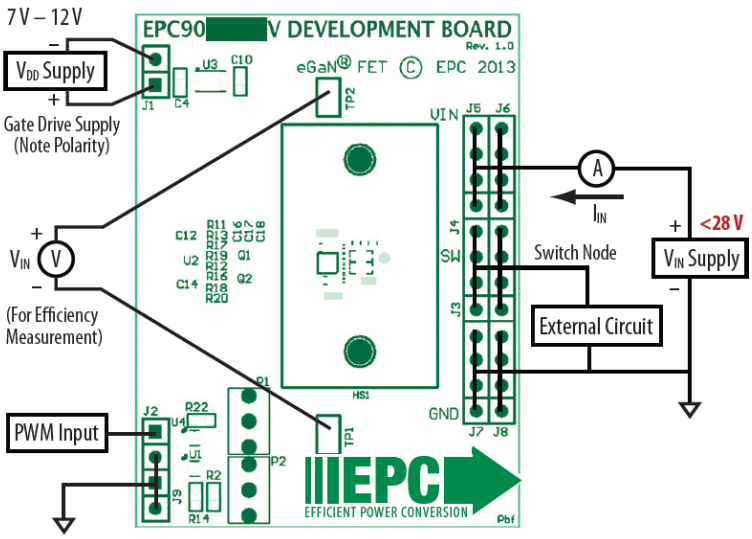


Figure 3.3 Proper connection and measurement setup of the evaluation board [31]

3.2 The Interface Board

Figure 3.4 depicts the schematic of the interface board. The interface board consists of two parts: the output stage of the buck converter and the voltage divider. The board is

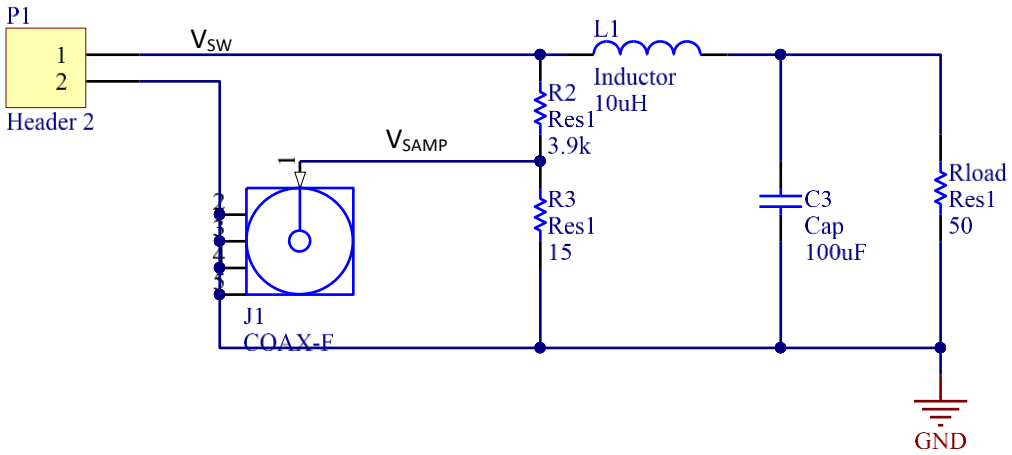


Figure 3.4 Schematic of the interface board

connected to the evaluation board with two headers (Header 2 in the schematic). The output of the interface board is the scaled down voltage V_{SAMP}. It is fed to the next stage with an SMA female connector.

3.2.1 The Output Stage of Buck Converter

In Figure 3.4, the inductor (L1), capacitor (C3) and the load resistor build up the output stage of the buck converter. Figure 3.5 is the simplified schematic of the buck converter. Additional circuits such as driver and dead time adjustment are not shown in this picture. The gate control signal of the GaN FETs is a 1MHz Pulse Width Modulation (PWM) signal with a duty cycle of 3%, in order to convert the 40V DC input to a 1.2V DC output.

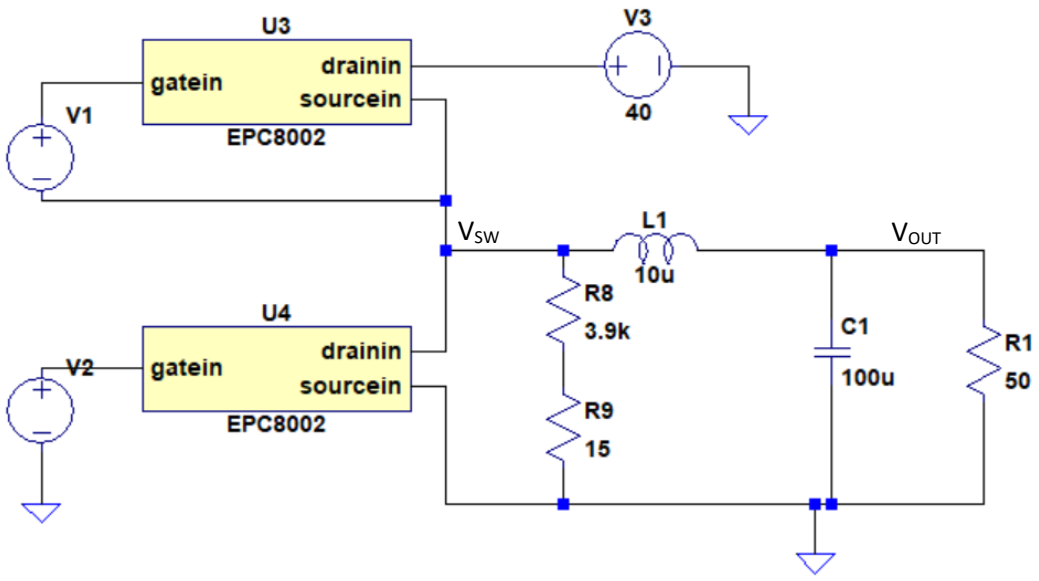


Figure 3.5 Schematic of the buck converter (simplified)

The simulation result from LTspice is plotted in Figure 3.6. It shows the output is 1.2V when the voltage is steady. The converter is working in CCM mode since the current passing the inductor is always above 0.

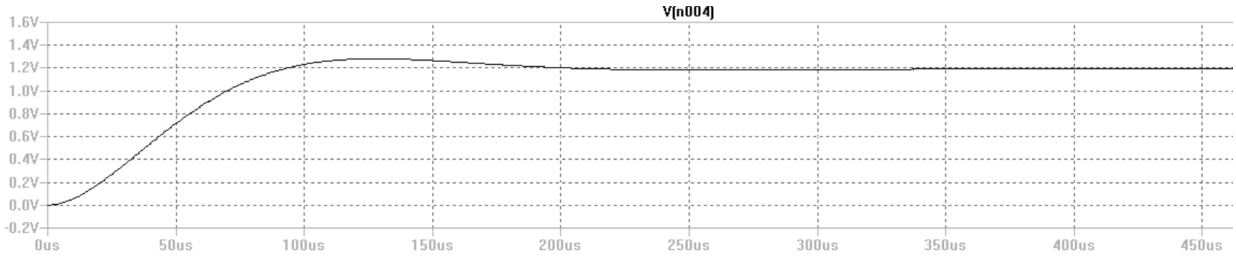


Figure 3.6 Simulation result of the buck output voltage

3.2.2 The Voltage Divider

The voltage divider is used to degrade the switching node voltage to meet the requirement of the ADC input. The ADC's maximum input value is around 500mV differential. Hence, we need to scale down the V_{SW} to around 250mV in amplitude. Both simple resistive divider and capacitive divider can scale down the voltage theoretically. However, the PCB testing result indicates that capacitive divider doesn't work as well as the resistive one in our case. As a result, a divider consists of two resistors is implemented here.

In the simulation, the components are all ideal so there is no interference in the circuit by stray capacitors and inductors. The final waveform is quite clean as we can see in Figure 3.7. Nevertheless, due to the EMI effect, the switching node voltage always has an overshooting problem so the maximum value could reach 50~60V instead of 40V. Therefore, high voltage resistors are selected for voltage divider. In this case, we are

using a 3.9kΩ resistor and a 12Ω resistor both with 0805 package. They can degrade the 40V input to 120mV as simulated in Figure 3.8.

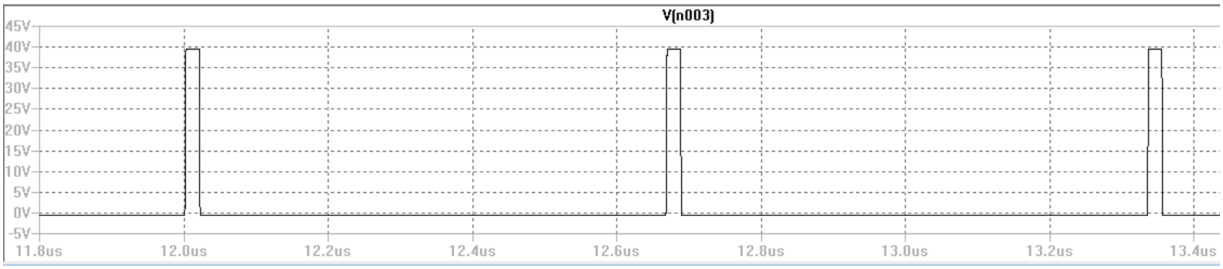


Figure 3.7 Simulation result of the switching node voltage

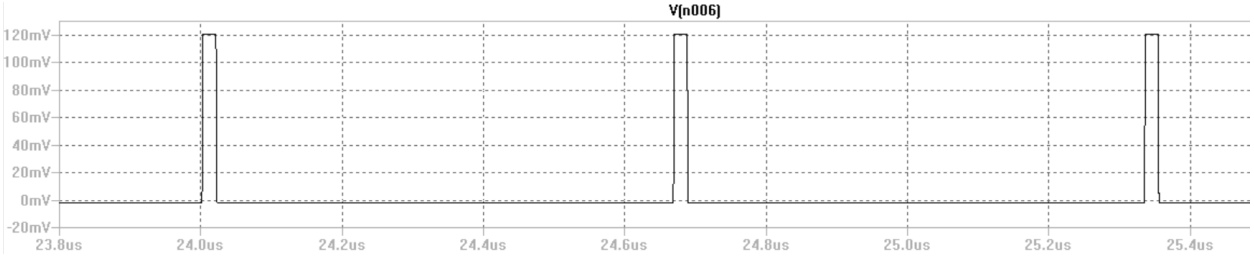


Figure 3.8 Simulation result of the voltage divider

These sensing resistors and the parasitic capacitor of the chip's pad can form a low pass filter at the input of the ADC. The model of this filter can be depicted by Figure 3.9. The parasitic capacitor of this chip is about 200fF. By calculation, the cut-off frequency of this filter is $\frac{\frac{R1+R2}{CR1R2}}{2\pi}$. In our case it is 66.52GHz, which is a lot higher than the Nyquist frequency (500MHz). So there is no need to worry about this filter may filter out some of the frequency components.

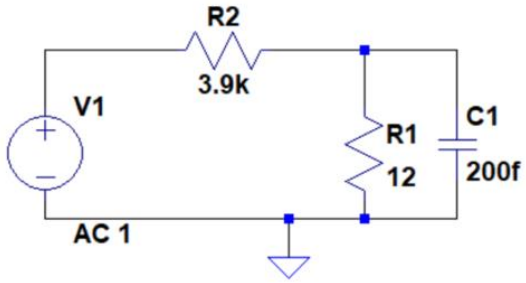


Figure 3.9 Low pass filter model

3.2.3 PCB Design of the Interface Board

For high-speed operations, parasitic components of a device are critical to the circuit. In order to minimize the influence of the parasitic inductors and capacitors, the components of the interface board are all SMT devices with 0805 package. Also, to minimize the stray inductors and capacitors of wires, a PCB is designed instead of soldering components onto a perfboard, as shown in Figure 3.10. The size of the PCB is not optimized because it is difficult to solder by hand if the PCB is too small.

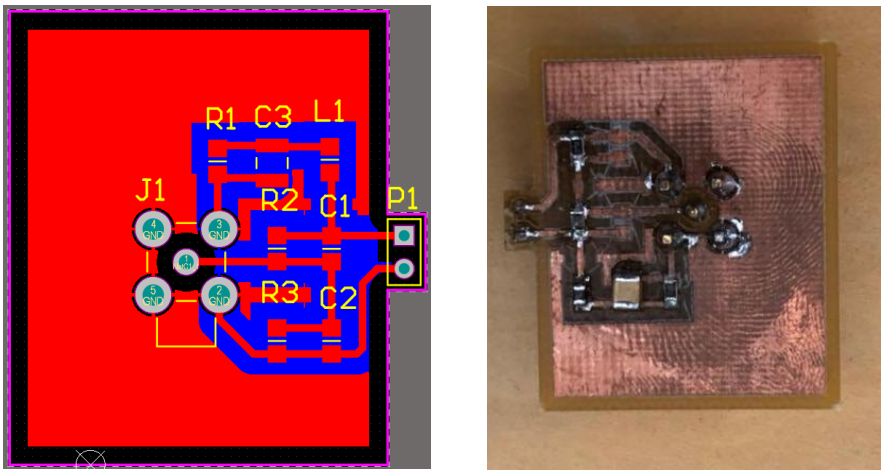


Figure 3.10 PCB design of the interface board

Using the fabrication machine on campus, a PCB prototype is produced.

3.3 ADC Sensing Set-up

In order to perform the ADC sensing correctly, the ADC needs to be accurately configured. The rectangular box in Figure 3.11 depicts the ADC sensing setup.

3.3.1 Single-ended to Differential Converter

Before feeding the V_{SAMP} to the ADC for measurement, a single-ended to differential signal converter is implemented.

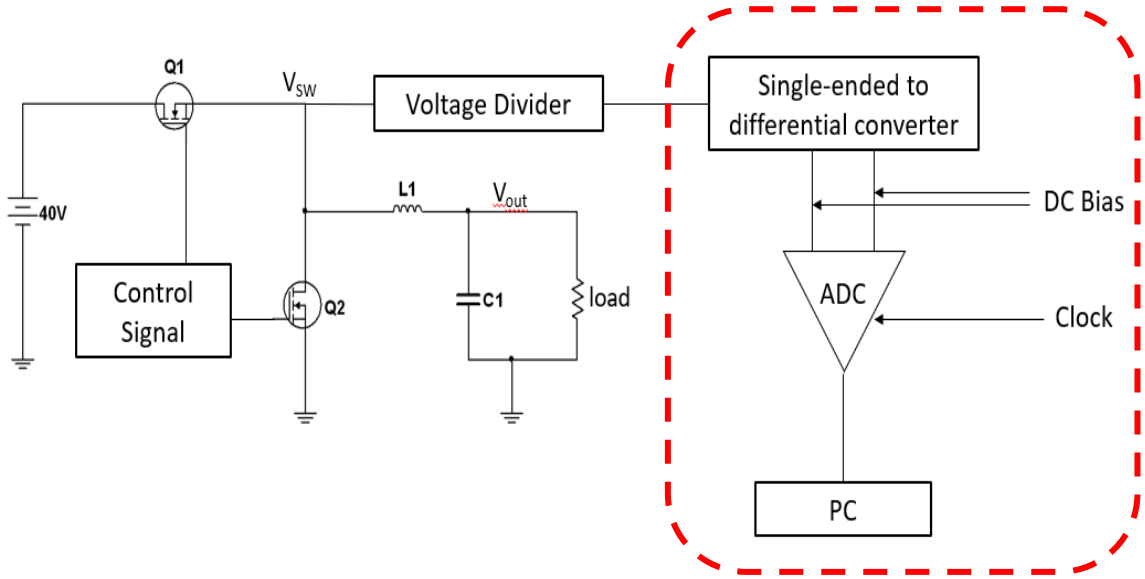


Figure 3.11 ADC sensing setup

There are two options for this converter: op-amp-based converter and balanced-to-unbalanced (balun) circuit.

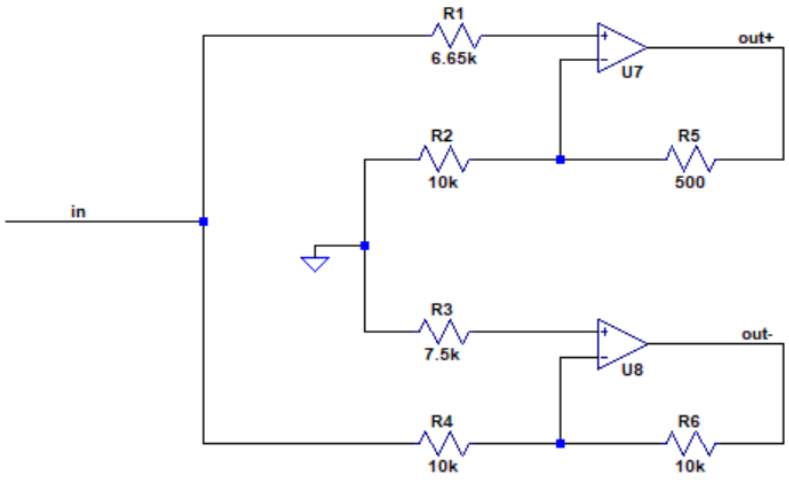


Figure 3.12 Schematic of op-amp based converter

For the op-amp-based converter, utilizing two op-amps (Figure 3.12) could produce a neat differential signal as plotted in Figure 3.13. However, most of the op-amps can not support a very high frequency. The simulation result in Figure 3.13 is based on ideal devices.

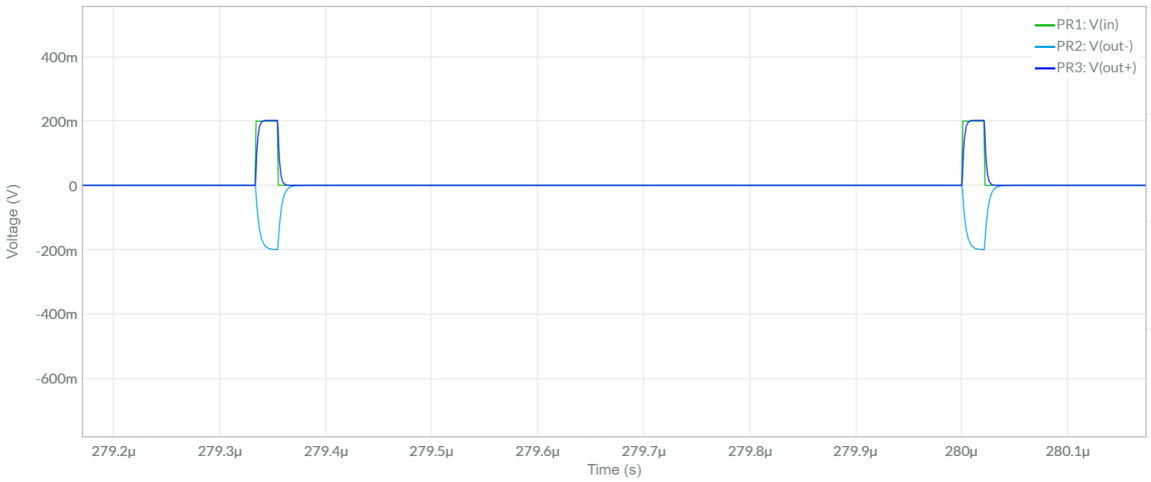


Figure 3.13 Simulation result of the single-ended to differential converter

Therefore, in this project we use a pre-manufactured balanced-to-unbalanced circuit (balun) as a single-ended to differential signal converter.

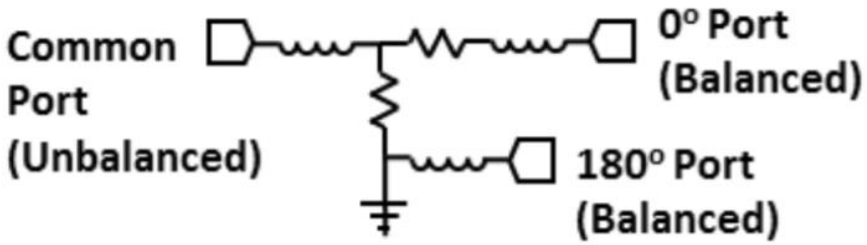


Figure 3.14 Balun

A balun is a three-port device which splits the input into two outputs (Figure 3.14). Two outputs have the opposite signals, which means they have a 180° phase shift in phase domain. Since it can transform the input signal into two signals that is negative to each other, it is able to convert a single-ended signal to differential ones.

Figure 3.15 Marki Bal-0036

3.3.2 Communication Between ADC and PC

The communication between ADC and PC is based on the ADC's motherboard. The motherboard contains a pre-programmed controller to realize the signal transport from

the on-chip memory to the computer using UART protocol with the following parameters.

Table 3.1 Communication Parameters

Parameter	**Value**
Baud Rate	115200
Data Bits	8
Stop Bits	1
Parity	No Parity

The connection between the motherboard and the computer is shown in Figure 3.16.

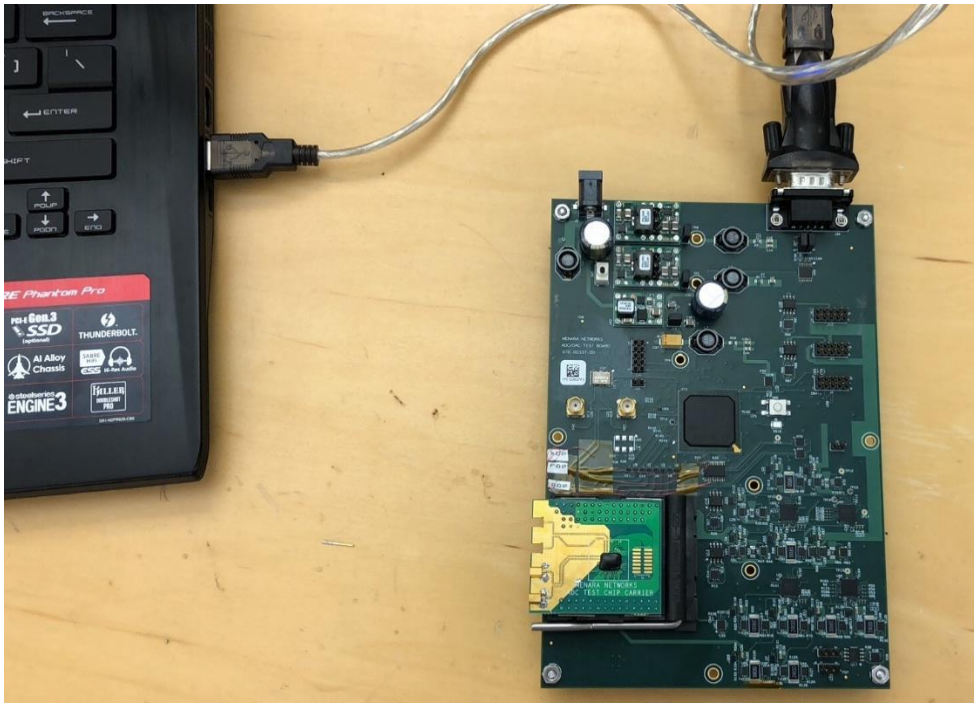


Figure 3.16 Connection between motherboard and PC

CHAPTER 4
TESTING RESULTS

Testing result of the ADC sensing strategy is discussed in this chapter.

4.1 Testing of the Interface Board

After soldering the interface board, testing of the design is implemented. Figure 4.1 shows the buck converter with the evaluation board and the interface board. Given the specific input signals, the buck is first measured by oscilloscope to verify that it can work properly.

Figure 4.2 depicts the output of the buck converter. It is a rather clean constant voltage at 1.2V, which meet the requirement as a buck converter. (Comparing with Figure 3.6)

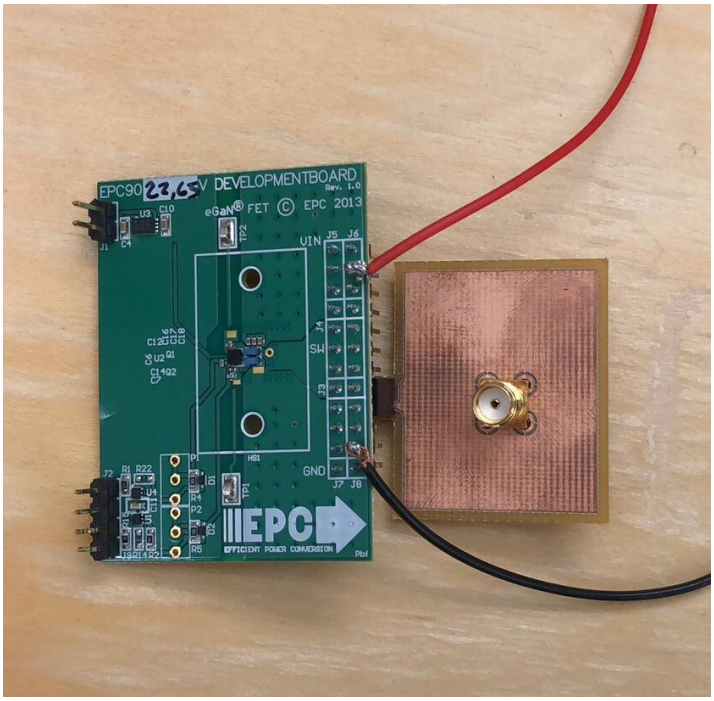


Figure 4.1 Buck Converter

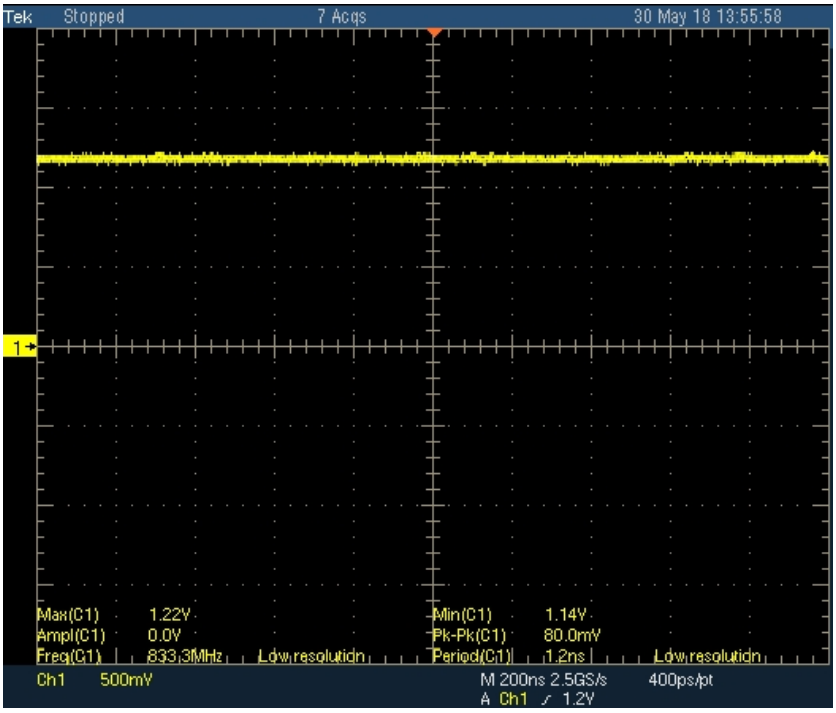
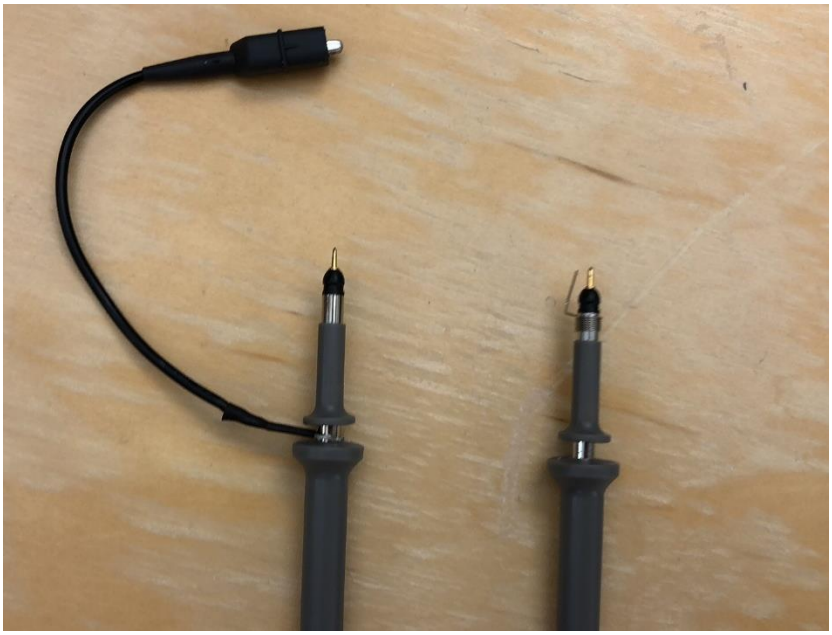


Figure 4.2 Waveform of the buck output

While measuring the output voltage and switching node voltage with oscilloscope, extra cares should be taken for the probes. The standard 3-inch long ground wire (Figure 4.43(a)) of the probe needs to be avoided because the long wire loop will act as an antenna by picking up any radiated noise from the evaluation board, which can increase the peak value of the overshooting [6]. The short ground lead in Figure 4.3(b) is the right one to choose in this measurement.



(a) (b)

Figure 4.3 Two types of oscilloscope probe's ground wire

For the input to the ADC, the divider's output is in Figure 4.4. The testing result in the picture below is the subtraction of the two balun outputs.

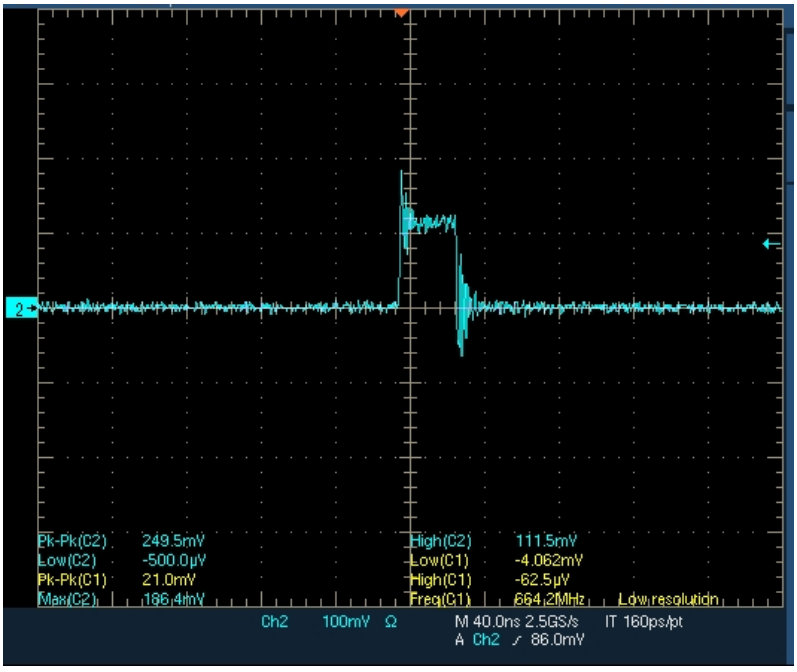


Figure 4.4 Testing result of the V_{SAMP}

With the help of a signal analyzer, the spectrum of the switching node voltage can be observed (Figure 4.5).

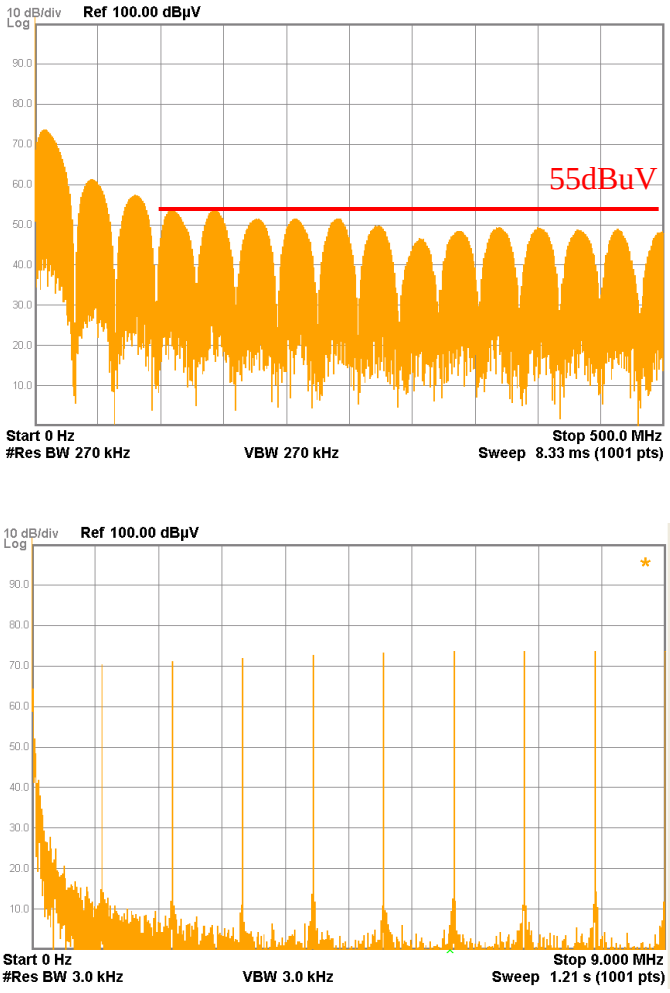


Figure 4.5 Spectrum of the Vsw (second plot is zoomed in)

For comparison, a switching node voltage with larger ringing is generated for measurement. Figure 4.6 shows its time domain waveform.

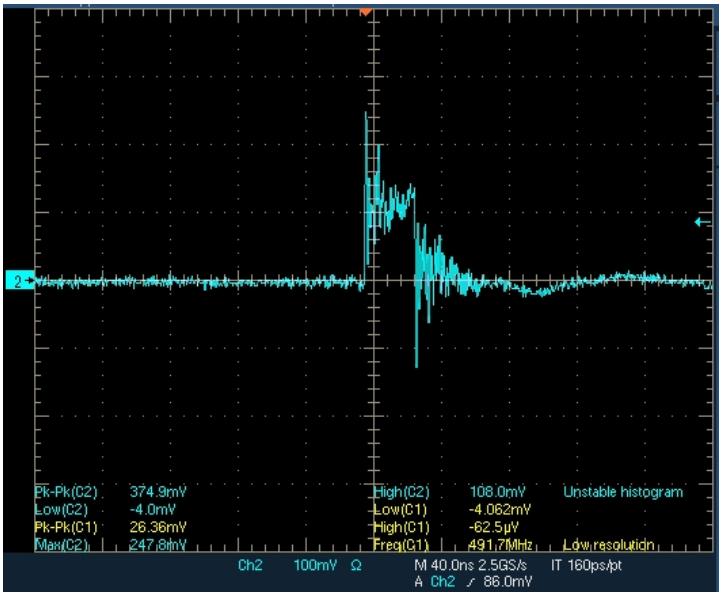


Figure 4.6 Testing result of the V_{SAMP} (large ringing)

The spectrum is displayed in Figure 4.7. This result indicated that the amplitude of spectrum didn't change much at lower frequency but increased by about 5dBuV at high frequency when a larger ringing appeared at the switching node.

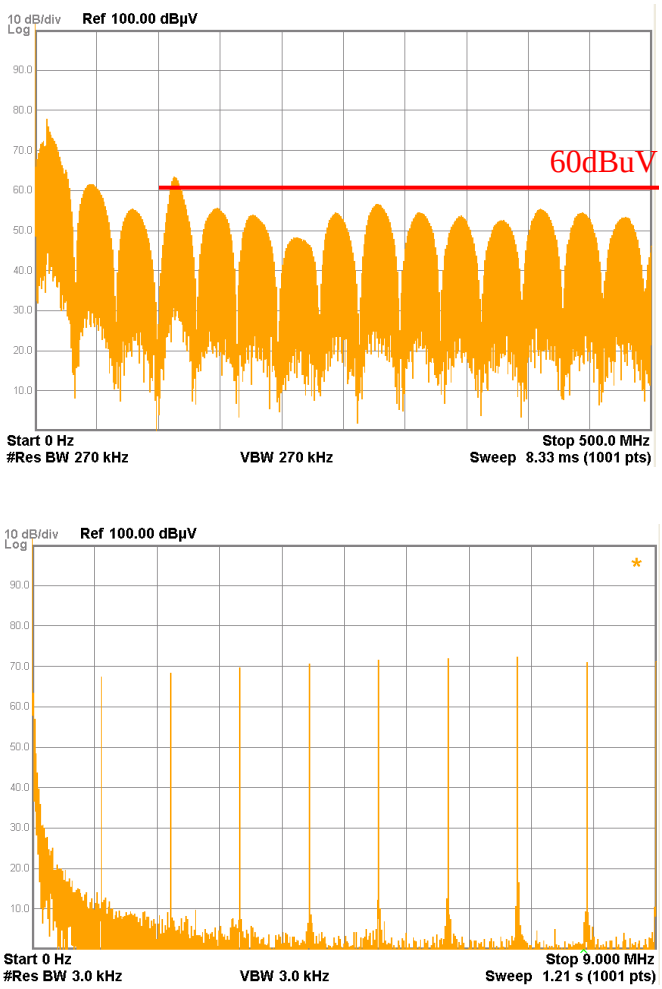


Figure 4.7 Spectrum of the V_{SW} with larger ringing (second plot is zoomed in)

4.2 ADC Sensing Result

After connecting the ADC with correct signal inputs and outputs as illustrated in Figure 4.8, the ADC sensing can be performed on the PC. If the sensing result of the ADC is similar to the results in section 4.1, then the proposed EMI evaluation method is feasible.

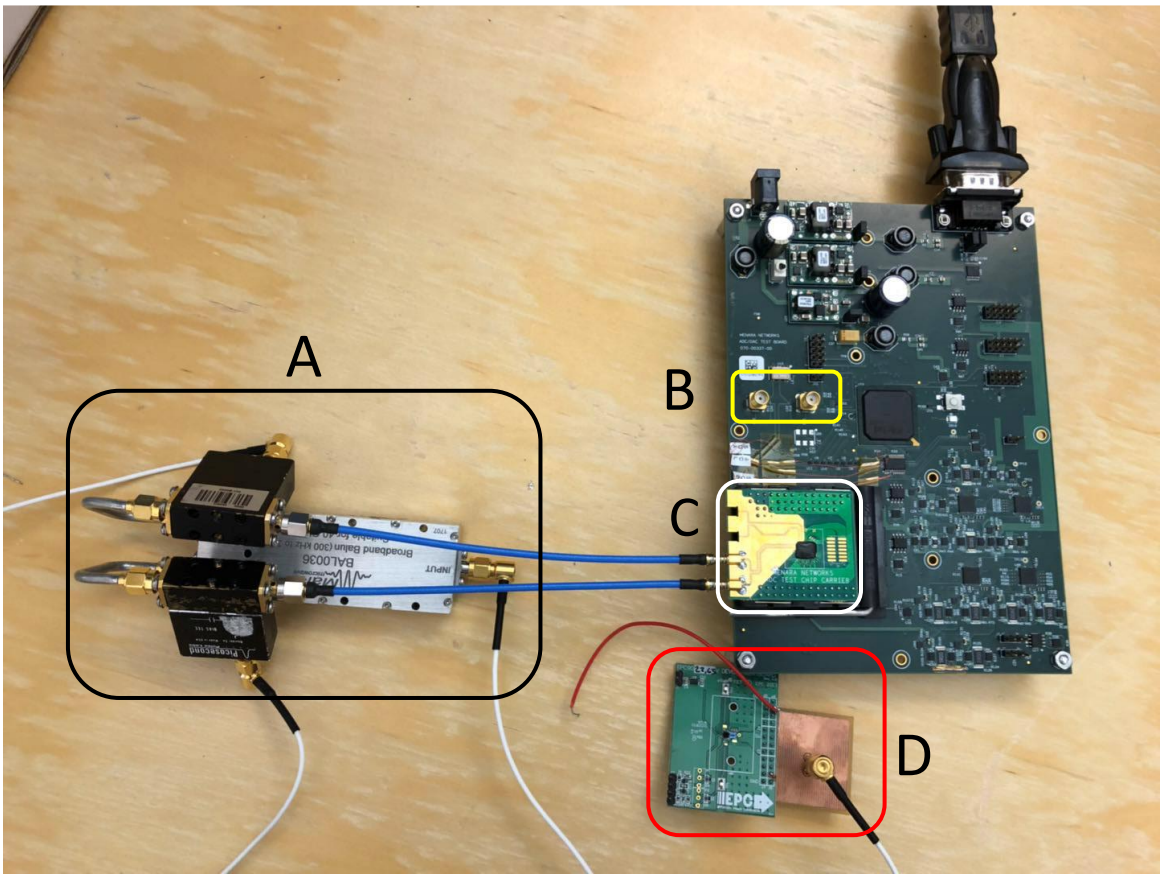


Figure 4.8 Overall measuring setup. A: balun with bias-Tees, B: external clock, C: ADC chip, D: buck converter

The control of the motherboard's controller is realized by the software Tera Term. The ADC can sample 16 cycles (16.75us) of the input data each time. The testing result of ADC returns as digital data as shown in Figure 4.9.

```
0 4000 3b
0 4001 d5
0 4002 1c7
0 4003 7f
0 4004 3f
0 4005 d5
0 4006 1cf
0 4007 7f
0 4008 1cf
0 4009 7f
0 400a 1c7
0 400b 7f
0 400c 1cf
0 400d 7f
0 400e 1c7
0 400f 7f
0 4010 3f
0 4011 d5
0 4012 1cf
0 4013 7f
0 4014 1cf
0 4015 7f
0 4016 1cf
0 4017 7f
0 4018 1cf
0 4019 7f
0 401a 1c3
0 401b 7f
```

Figure 4.9 Part of digital data

The digital information is then processed by MATLAB on computer to achieve the actual waveform of the switching node voltage. Figure 4.10 and 4.11 are the time domain waveform sampled by the ADC with different ringing level. Comparing with Figure 4.4 and 4.6, these results are almost identical to each other.

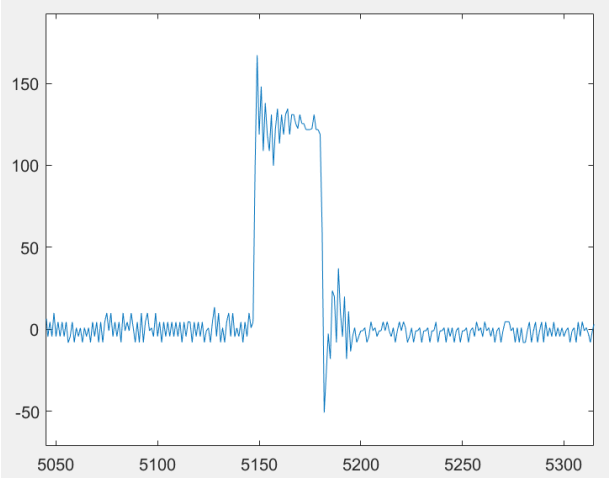


Figure 4.10 ADC measured V_{SW} (small ringing)

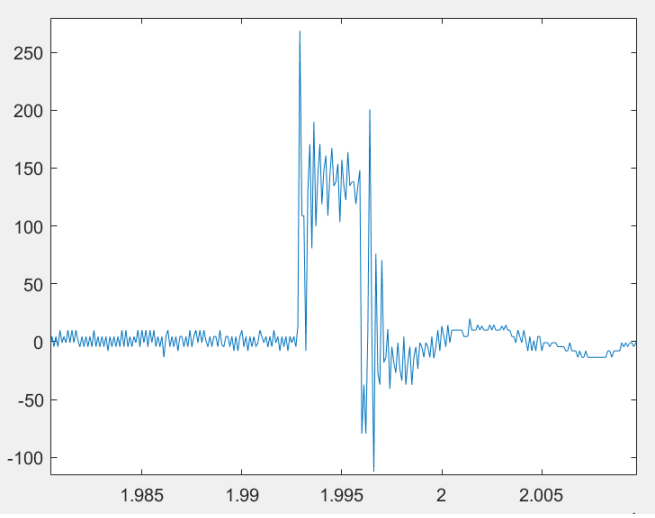


Figure 4.11 ADC measured V_{SW} (large ringing)

The spectrum can also be obtained with MATLAB (Figure 4.12 and 4.13). The spectrum is quite similar to the testing results with signal analyzer in Figure 4.5 and 4.7. Although they are not exactly the same, the frequency domain information is still good enough for the evaluation of EMI level because the change in magnitude can be observed when the ringing level is varying. The 5dBuV drop on the magnitude can easily be noticed from the ADC result.

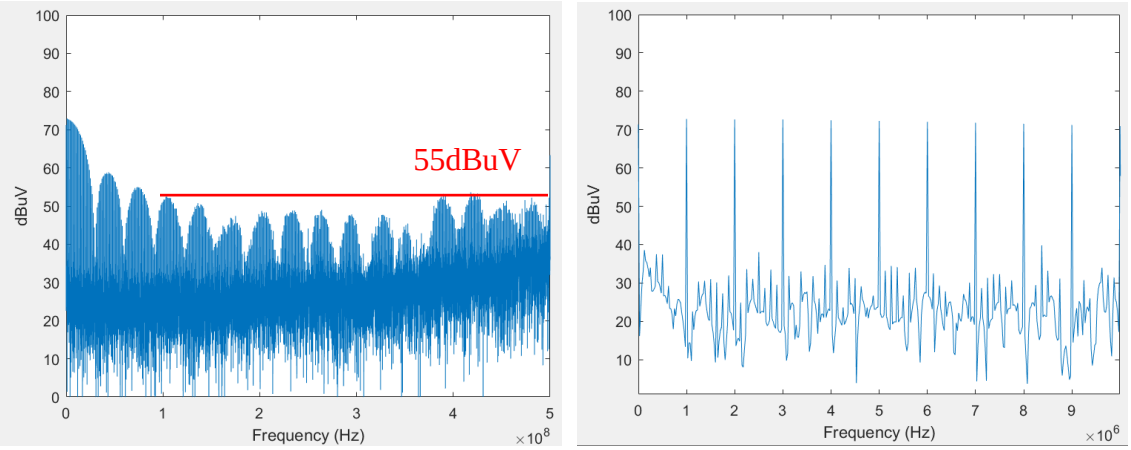


Figure 4.12 Spectrum of the Vsw (second plot is zoomed in)

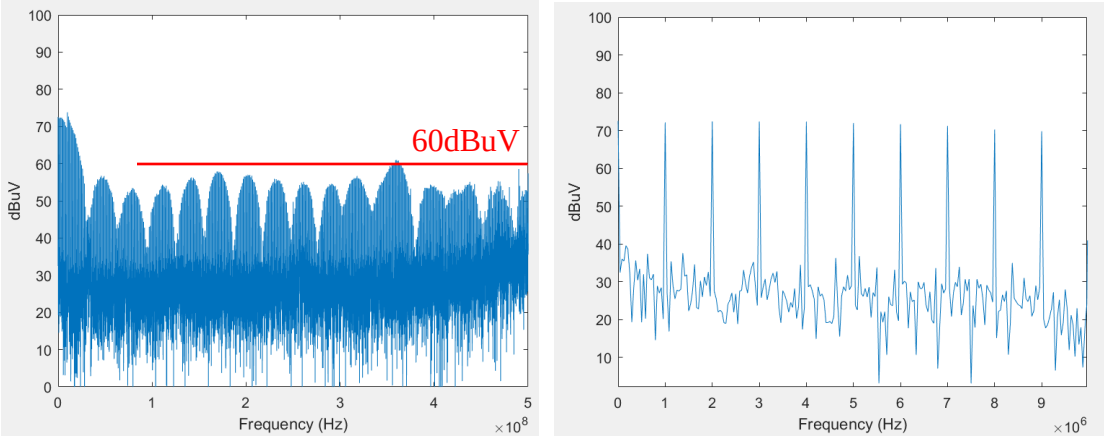


Figure 4.13 Spectrum of the V_{SW} with large ringing (second plot is zoomed in)

CHAPTER 5
SUMMARY

In this thesis, an ADC-based EMI evaluation scheme on GaN device was verified.

By comparing the sensing results of the ADC to the equipment measured results demonstrated in Chapter 4, it appears that two sets of data are almost identical so that we can assess the EMI level with the ADC measured switching node voltage. Therefore, the conclusion can be drawn that it is feasible to evaluate the EMI of GaN-based power converters with a high-speed ADC.

The proposed evaluation method has the following advantages:

a. The ADC sensing strategy could provide detailed information about the ringing in both time domain and frequency domain.
b. High-speed evaluation by the ADC offers the possibility to provide the control signals for the gate current control drivers.
c. The sensing set up is quite simple, so it is easy to change the evaluation point (e.g. input DC voltage) to evaluate different types of EMI.

For the future development of this project, this method of EMI evaluation can be used for active GaN FET driver design. The driver can adjust its driving strength based on the evaluation result from the ADC in order to optimize the switching activity, which would greatly improve the performance of the GaN device drivers.

BIBLIOGRAPHY

[1] Baliga, B. J. (2010). *Fundamentals of power semiconductor devices*. Springer Science & Business Media.

[2] Mitani, E., Haematsu, H., Yokogawa, S., Nikaido, J., & Tateno, Y. (2006, April). Mass production of high voltage GaAs and GaN devices. In *CS Mantech Conference* (pp. 24-27).

[3] van Roy, R. (2016). Reducing EMI in buck converters. *Application Note, Richtek Technology Corporation*.

[4] Mainali, K., & Oruganti, R. (2010). Conducted EMI mitigation techniques for switch-mode power converters: A survey. *IEEE Transactions on Power Electronics*, *25*(9), 2344-2356.

[5] Ke, X., Sankman, J., Chen, Y., He, L., & Ma, D. B. (2017, February). 25.2 A 10MHz 3-to-40V V IN tri-slope gate driving GaN DC-DC converter with 40.5 dBμV spurious noise compression and 79.3% ringing suppression for automotive applications. In *Solid-State Circuits Conference (ISSCC), 2017 IEEE International* (pp. 430-431). IEEE.

[6] Texas Instrument. (2011). Ringing reduction techniques for NexFET high performance MOSFETs. *Texas Instrument., Application Report*. SLPA010.

[7] Wilson, T. G. (2000). The evolution of power electronics. *IEEE Transactions on Power electronics*, *15*(3), 439-446.

[8] Majumdar, G. (2004, June). Future of power semiconductors. In *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual* (Vol. 1, pp. 10-15). IEEE.

[9] Iwamuro, N., & Laska, T. (2017). IGBT history, state-of-the-art, and future prospects. *IEEE Transactions on Electron Devices*, *64*(3), 741-752.

[10] Mishra, U. K., Shen, L., Kazior, T. E., & Wu, Y. F. (2008). GaN-based RF power devices and amplifiers. *Proceedings of the IEEE*, *96*(2), 287-305.

[11] Jones, E. A., Wang, F. F., & Costinett, D. (2016). Review of commercial GaN power devices and GaN-based converter design challenges. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, *4*(3), 707-719.

[12] Ozpineci, B., & Tolbert, L. M. (2004). *Comparison of wide-bandgap semiconductors for power electronics applications*. United States. Department of Energy.

[13] Asbeck, P. M., Yu, E. T., Lau, S. S., Sullivan, G. J., Van Hove, J., & Redwing, J. (1997). Piezoelectric charge densities in AlGaN/GaN HFETs. *Electronics letters*, *33*(14), 1230-1231.

[14] Dadgar, A., Schulze, F., Wienecke, M., Gadanecz, A., Bläsing, J., Veit, P., ... & Krost, A. (2007). Epitaxy of GaN on silicon—impact of symmetry and surface reconstruction. *New Journal of Physics*, *9*(10), 389.

[15] Colino, S. L., & Robert A. Beach, R.A. Fundamentals of Gallium Nitride Power Transistors. *Application Note*. Efficient power conversion.

[16] Huang, X., Liu, Z., Li, Q., & Lee, F. C. (2014). Evaluation and application of 600 V GaN HEMT in cascode structure. *IEEE Transactions on Power Electronics, 29*(5), 2453-2461.

[17] Mohan, N., & Undeland, T. M. (2007). *Power electronics: converters, applications, and design*. John Wiley & Sons.

[18] Nowakowski, R., & Tang, N. (2009). Efficiency of synchronous versus nonsynchronous buck converters. *Texas Instruments Incorporated*.

[19] Erickson, R. W., & Maksimovic, D. (2007). *Fundamentals of power electronics*. Springer Science & Business Media.

[20] Li, Z., & Pommerenke, D. (2005, August). EMI specifics of synchronous DC-DC buck converters. In *Electromagnetic Compatibility, 2005. EMC 2005. 2005 International Symposium on* (Vol. 3, pp. 711-714). IEEE.

[21] Rohm Semiconductor. (2016). Snubber Circuit for Buck Converter IC: Power Management. *Rohm Semiconductor*. Application Note.

[22] Kam, K. W., Pommerenke, D., Lam, C. W., & Steinfeld, R. (2008, August). EMI analysis methods for synchronous buck converter EMI root cause analysis. In *Electromagnetic Compatibility, 2008. EMC 2008. IEEE International Symposium on* (pp. 1-7). IEEE.

[23] IEC61000: Electromagnetic Compatibility, 2000.

[24] CISPR25: Limits and methods of measurement of radio disturbance characteristics for the protection of receivers used on board vehicles.

[25] Reby, F., Bausiere, R., Sohier, B., & Costa, F. (1998, September). Reduction of radiated and conducted emissions in power electronic circuits by the continuous derivative control method (CDCM). In *Power Electronics and Variable Speed Drives, 1998. Seventh International Conference on (Conf. Publ. No. 456)* (pp. 158-162). IET.

[26] Yang, X., & Palmer, P. R. (2013, September). Shaping pulse transitions by active voltage control for reduced EMI generation. In *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE* (pp. 1682-1687). IEEE.

[27] Oswald, N., Stark, B. H., Holliday, D., Hargis, C., & Drury, B. (2011). Analysis of shaped pulse transitions in power electronic switching waveforms for reduced EMI generation. *IEEE Transactions on Industry Applications*, *47*(5), 2154-2165.

[28] Wang, J., Liu, D., Dymond, H. C., Dalton, J. J., & Stark, B. H. (2017, October). Crosstalk suppression in a 650-V GaN FET bridgeleg converter using 6.7-GHz active gate driver. In *Energy Conversion Congress and Exposition (ECCE), 2017 IEEE* (pp. 1955-1960). IEEE.

[29] Wang, G., Sun, K., Zhang, Q., Elahmadi, S., & Gui, P. (2017, September). A 43.6-dB SNDR 1-GS/s single-channel SAR ADC using coarse and fine comparators with background comparator offset calibration. In *ESSCIRC 2017-43rd IEEE European Solid State Circuits Conference* (pp. 175-178). IEEE.

[30] Yoo, A., Chang, M., Trescases, O., Wang, H., & Ng, W. T. (2007, December). FOM (Figure of Merit) Analysis for Low Voltage Power MOSFETs in DC-DC Converter. In *Proc. IEEE Conf. Electron Devices Solid-State Circuits (EDSSC)* (pp. 1039-1042).

[31] A. Lidow. Demonstration Board EPC9022/23/24/25/27/28/29/30 Quick Start Guide. EPC