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High-Speed Successive Approximation Register (SAR) ADC Design with Multiple Concurrent Comparators

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HIGH-SPEED SUCCESSIVE APPROXIMATION REGISTER (SAR) ADC

DESIGN WITH MULTIPLE CONCURRENT COMPARATORS

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High-speed Successive Approximation Register (SAR) ADC
Design with Multiple Concurrent Comparators

Advisor: Professor Ping Gui

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High-performance integrated Analog-to-Digital Converters (ADC) play an indispensable role in digital processing since they are the interface circuits that bridge the analog world and digital regime. Successive Approximation Register (SAR) ADCs have been gaining more interests in recent years due to their power efficiency and digital friendliness. However, the conversion speed of SAR ADCs is less competitive than other ADC architectures because of its binary search mechanism. This study presents a 400MS/s 8-bit SAR ADC using multiple concurrent comparators to enhance the conversion speed. Additionally, CMOS T/H circuit and dummy switch are also implemented to increase linearity and compensate charge injection. SAR logic is improved in addition to increase the conversion speed further. Simulation results have shown the effectiveness of the proposed SAR ADC. The proposed design is designed in 65nm CMOS technology and achieves an SNDR of 44dB at 400MS/s for a Nyquist input while consuming 530μW.

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Introduction

High-performance integrated Analog-to-Digital Converters (ADCs) play an indispensable role in digital processing since they are the interface circuits that bridge the analog world and digital regime. Successive Approximation Register (SAR) ADCs have been gaining more interest in recent years due to their power efficiency and digital friendliness. The well-defined digital signals propagate more efficiently than analog signals because it is easier for electronic circuits to distinguish '0's and '1's from noise. As a result, digital signal processing is ubiquitous in electronic industries, such as wireless communications and biometric sensor systems, where analog signal is required to be converted and processed in digital form. High-performance integrated Analog-to-Digital Converters are interface circuits that bridge the analog world and digital regime. For instance, in the receiver path of a wireless transceiver system shown in Figure 1.1, the antenna senses the input analog signal which is amplified by the subsequent Low Noise Amplifier (LNA). Then the mixer driven by an on-chip oscillator down-converts the amplified signal. At last, the ADC following the bandpass filter transfers the intermediate frequency signal into digital codes. In the receiving end, the ADC speed is critical since it directly determines the efficiency of digital signal processing. As the data rate of wireless communication increases in recent years, ADCs used in the system are pushed toward higher conversion speed.

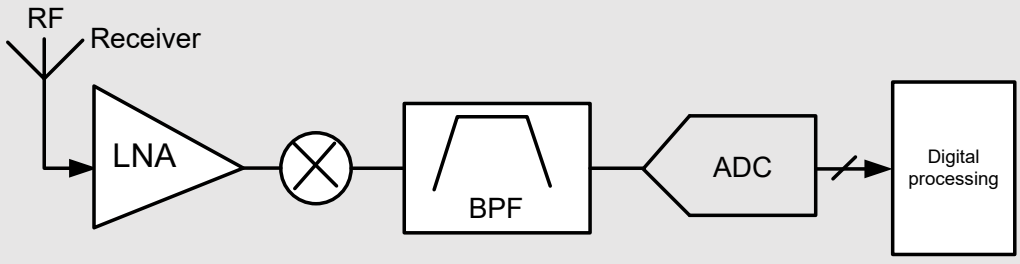

Figure 1.1 Receiver path of wireless transceiver system

Moreover, power consumption is another main concern in ADC designs since an increasingly number of data-acquisition applications are designed to be battery-powered and consume as little power as possible while performing necessary functions. The key contributor to achieving that is the adoption of low power and scaling friendly ADC architectures. Successive Approximation Register (SAR) ADCs are well known for their power efficiency because most building blocks consume dynamic power and SAR ADCs are compatible with deeply scaled complementary metal oxide semiconductor (CMOS) technologies. However, due to its binary search mechanism, SAR ADCs need many steps to process a single analog data, resulting in inherently lower speed compared to other architectures, such as flash ADCs, which finish the conversion by only one step.

A lot of research has been done in the past decade to improve the performance of SAR ADCs. For example, an asynchronous SAR ADC was proposed in [1] to remove the high-speed internal clock and increase the conversion speed. But a single comparator is utilized to execute multiple comparisons, so the ADC speed is still limited since the comparator needs to be reset repetitively. In order to remove the comparator reset time, this thesis presents an 8-bit SAR ADC using multiple concurrent comparators. Because each comparator is activated before the previous one is reset completely, the conversion speed is improved. The proposed design is implemented in 65nm CMOS technology and achieves an SNDR of 44dB at 400 Mega samples per second (MS/s) for a Nyquist input while consuming 530μW. With time-interleaving technique, the ADC can achieve gigahertz range of sampling, which is the requirement for many applications, such as serial link transceivers and wireless communication systems [2]. The remaining part of the thesis is organized as follows: Chapter 2 describes ADC performance metrics and different types of ADC. Chapter 3 introduces the proposed SAR ADC structure and compares it to the conventional SAR ADC architecture. Chapter 4 elaborates the design considerations and shows the simulation results. At last, the conclusion and the future work are included in Chapter 5.

Chapter 2

Fundamentals of ADC

ADCs convert analog signals into digital outputs and the process can be divided into two parts: sampling and quantization [3]. Sampling is a process of taking samples from a varying analog signal. Figure 2.1 depicts the model of a sampling circuit. The switch S_0 being closed enables the voltage node V_1 to follow the analog signal V_0 under a certain bandwidth restriction. When S_0 is open, the sampled analog value V_1 is kept in the capacitor C_0.

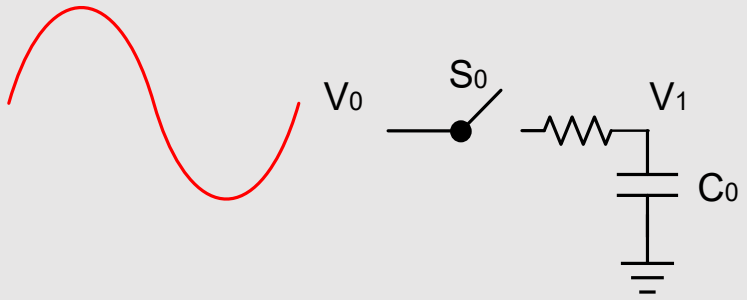

Figure 2.1 ADC sampling diagram

Quantization is a process of mapping the sampled value to the correct digital output. For an N-bit ADC, the largest input range (full-scale range) can be divided into 2^N identical segments. Each segment is called "quantization level", which corresponds to a distinct output of digital code. The width of each quantization level is defined as "Least Significant Bit" or LSB. Between two adjacent quantization levels is a reference voltage or reference threshold. ADCs compare the analog input with different reference thresholds to indicate which quantization level the input is located. Take a 3-bit ADC, shown in Figure

2.2, as an example. Eight even-space quantization levels are uniquely mapped to eight digital outputs (from “000” to “111”). The level where the input sits indicates the digital output (“110”). Because the analog sample is always rounded to a quantized value, we define “quantization error” (Δe) as the difference between the quantized value and the analog sample.

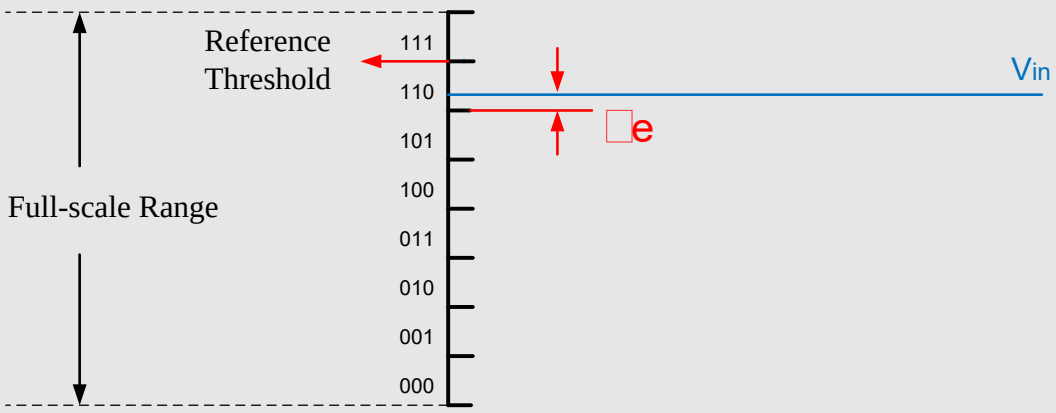

Figure 2.2 3-bit quantization

2.1 ADC Metrics

2.1.1 DNL (Differential Non-linearity)

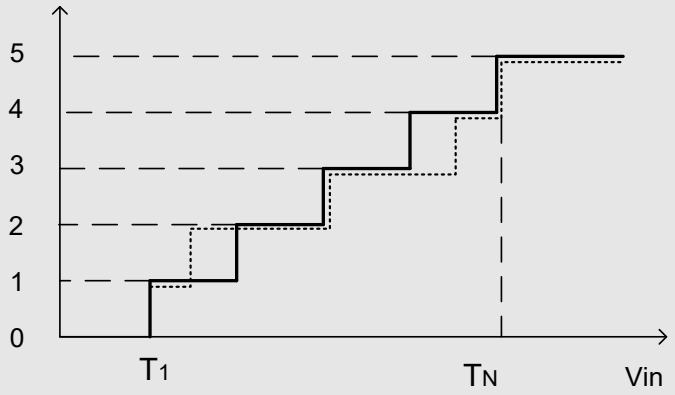

Figure 2.3 Difference between ideal and real code width

Figure 2.3 illustrates the transfer characteristics of an ADC. The solid curve is the ideal one where all digital codes have equal widths, while the dotted curve is realistic one representing

nonlinearity. T_1 and T_n are the first and the last transition voltage. For a N-bit ADC, the ideal code width can be derived:

$$W_{ideal} = \frac{T_N - T_1}{N - 1}$$

DNL is defined as the deviation of each real code width W_N with respect to the ideal code width W_{ideal}:

$$DNL_N = \frac{W_N - W_{ideal}}{W_{ideal}}$$

The first code width and the forth code are both half of W_{ideal}, leading DNL of the two codes to be -0.5 LSB; For the second and the third code, the actual width is one half longer than the ideal one, so the DNL is +0.5 LSB. Note that the first code (0) and the last code (5) are not defined with DNL. The DNL result of each code is plotted in Figure 2.4.

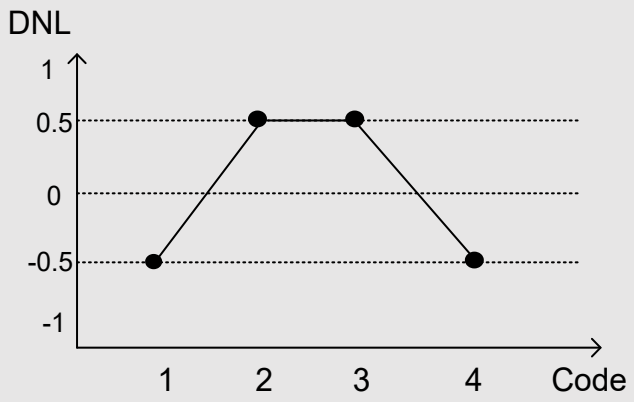

Figure 2.4 DNL chart of quantization

2.1.2 INL (Integral Non-linearity)

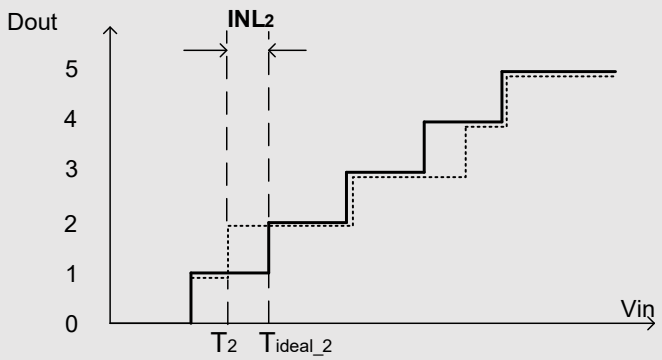

Figure 2.5 Transition difference between ideal and real ADC characteristics

In the ADC transfer characteristics, INL is defined as the deviation of each real transition voltage T_N with respect to the corresponding ideal transition voltage T_{ideal_N}:

$$INL_N = \frac{T_N - T_{ideal\_N}}{W_{ideal}}$$

In Figure 2.5, the second transition voltage and the second ideal transition voltage are labelled as T_2 and T_{ideal_2}. Since T_2 is smaller than T_{ideal_2} by $\frac{1}{2}W_{ideal}$, the INL for the second transition INL_2 is -0.5 LSB. The first and the third transition are ideal so INL_1 and INL_3 are both 0. Because the fourth transition voltage is greater than the ideal voltage by $\frac{1}{2}W_{ideal}$, INL_4 is 0.5LSB. The INL result is plotted in Figure 2.6.

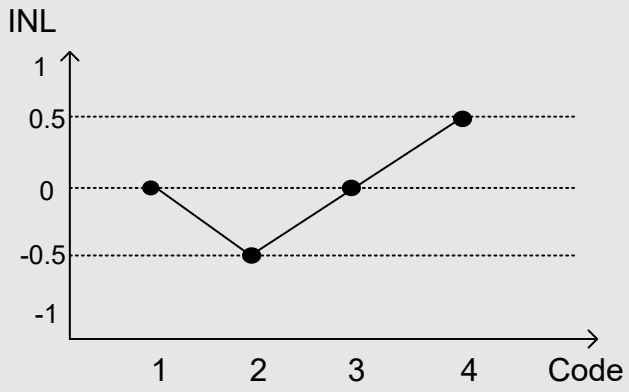

Figure 2.6 INL chart of quantization

2.1.3 SNR (Signal-to-Noise Ratio)

DNL and INL are static metrics since they are measured based on DC input voltages, which provide an understanding of ADC behaviors at low frequency. However, ADCs are also required to process high-frequency inputs and their performance have different specifications. A sinusoidal wave is typically used as an ADC's input to measure its performance. Its output is processed by FFT and represented in frequency domain.

The magnitude of an ADC input is half of the full-scale range and expressed as $\frac{2^N \times LSB}{2}$. The input signal power can be derived:

$$P_{signal} = \frac{1}{2}(\frac{2^N \times LSB}{2})^2$$

SNR is defined as the ratio of signal power P_{signal} to the system noise power P_{noise}:

$$SNR = 10\log\left(\frac{P_{signal}}{P_{noise}}\right)$$

Quantization noise $P_{noise,Q}$ is introduced by the ADC quantization error, and its power can be obtained as:

$$P_{noise,Q} = \frac{1}{12}LSB^2$$

In the ideal case when the system noise only includes the quantization noise, the SNR is also called SQNR (Signal-to-Quantization-Noise Ratio):

$$SQNR = 10\log\left(\frac{\frac{1}{2}\left(\frac{2^N \times LSB}{2}\right)^2}{\frac{1}{12}LSB^2}\right) = 6.02 \times \mathrm{N} + 1.76$$

2.1.4 SFDR (Spurious Free Dynamic Range)

Since the ADC input is a single-frequency signal, spectra of other frequencies generated at the ADC output are harmonics. SFDR is defined as the ratio of the signal power to the power of the maximum harmonic ($P_{harmonic,max}$).

$$\mathrm{SFDR} = 10\log\left(\frac{P_{signal}}{P_{harmonic,max}}\right)$$

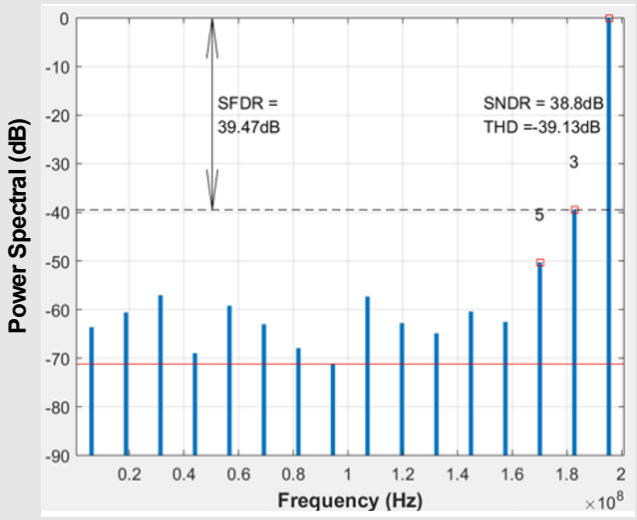

Figure 2.7 Frequency spectrum diagram

As depicted in the Figure 2.7, the strongest harmonic is the third harmonic, and the SFDR is 39.47dB

2.1.5 SINAD or SNDR (Signal-to-Noise-and-Distortion Ratio)

SNDR is defined as the ratio of the signal power to the total noise P_{noise} and harmonic power $P_{harmonic}$ in the system:

$$SNDR = 10\log(\frac{P_{signal}}{P_{noise} + P_{harmonic}})$$

2.1.6 ENOB (Effective Number of Bits)

In most cases, with a given ADC architecture and fixed power supply, the effective number of bits is fixed at a certain sampling clock [4]. SNDR is used to calculate the ENOB and their relationship is described as:

$$ENOB = \frac{SNDR - 1.76}{6.02}$$

2.2 Three basic types of ADC

2.2.1 Flash ADC

Flash ADCs are known for their ultra-fast speed. As shown in Figure 2.8, a flash ADC consists of a resistor-reference ladder, whose voltage nodes are connected to $2^N - 1$ comparators. In addition, a decoder is used to transfer comparators' outputs to binary digital outputs. The fast conversion speed of flash ADCs comes from the fact that the sampled input is compared with all reference thresholds at the same time. But since $2^N - 1$ comparators need to operate in parallel, high power consumption is a main drawback of this type of ADCs.

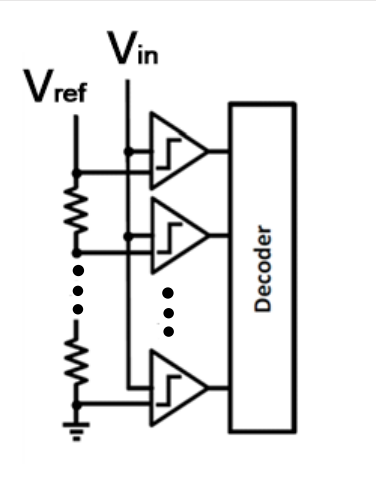

Figure 2.8 Flash ADC diagram

2.2.2 Pipeline ADC

The pipeline ADC is consisted of multiple stages, as depicted in Figure 2.9. Each stage contains a sub-ADC, a DAC and an amplifier. B bits of output quantized by the sub-ADC are fed to the DAC. The analog output is then subtracted from the sampled input, producing a residue voltage that is gained up by a factor of G and sent to the next stage. This gained-up residue continues through the pipeline, providing B bits per stage until it reaches the final stage. Note that when a stage finishes processing a sample and passing the residue to the next stage, it can then start processing the next sample, so the entireentire ADC works as a pipeline. An N-bit pipeline ADC only needs N comparators, consuming less power than the flash ADC, which incorporates $2^N - 1$ comparators. Moreover, because different pipeline stages process different analog samples concurrently, the conversion speed is only dependent on the speed of one stage. That is why pipeline ADC is also attractive for high speed applications. However, the linear processing of the analog input depends heavily on the accurate amplification, which is hard to achieve in scaled CMOS technologies. Additionally, the digital outputs of each stage are resolved at different times, so shift registers are needed to align all the bits, which complicates the logic design.

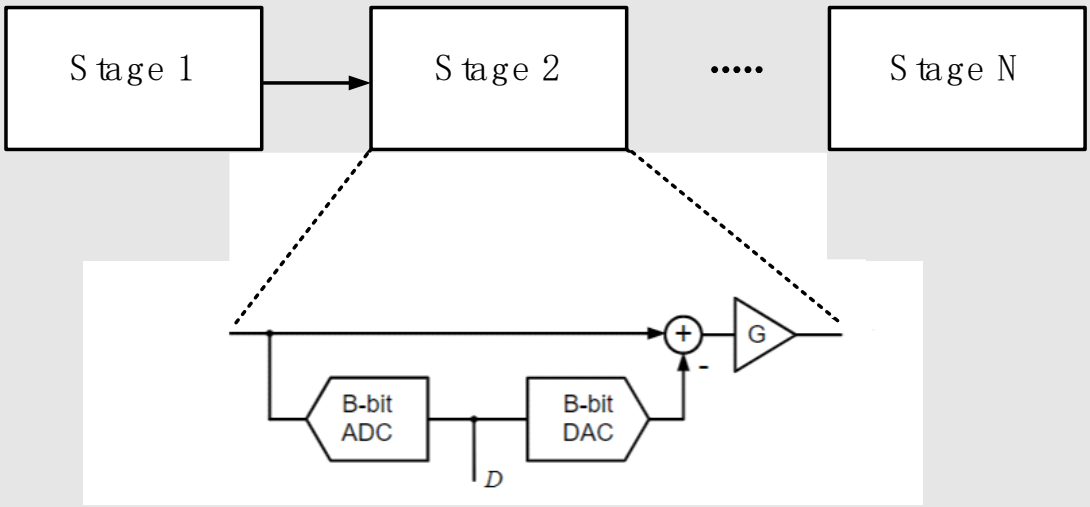

Figure 2.9 Pipeline ADC diagram

2.2.3 SAR ADC

SAR ADCs are the most power efficient ADCs among three architectures since they only utilize one comparator and do not need amplification stages. During quantization period, SAR ADCs use binary search mechanism to process analog signals. The mechanism is depicted in Figure 2.10. The searching range is the full-scale range at the beginning (from -1.2 to 1.2). The sampled input is first compared with the middle threshold of the range. Since the input (0.7) is greater than the threshold (0), the ADC yields "1" as the MSB output and the searching range is reduced to the upper half (from 0 to 1.2). Oppositely, if the input is smaller, the MSB output should be "0" and the searching range is narrowed to the lower half (-1.2 to 0). For the next cycle, the input is compared with the middle threshold of the updated searching range. Consequently, the second bit of output is yielded and the searching range is halved based on the comparison result. For N-bit SAR ADCs, the searching range is updated (N-1) times and N bits of the digital output are resolved.

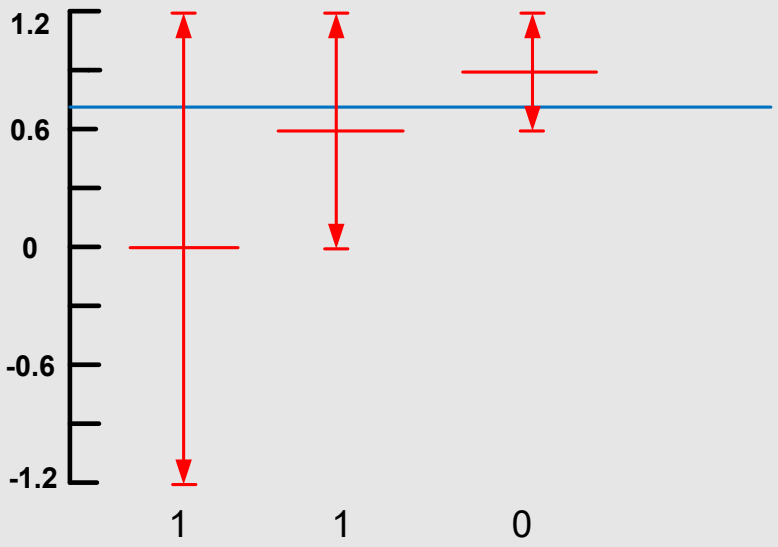

Figure 2.10 Binary search mechanism

As shown in Figure 2.11, a SAR ADC consists of four parts: Track/Hold circuit (T/H), Digital-to-Analog Converter (DAC), comparator and SAR logic. The Track/Hold circuit samples the continuously varying analog signal and holds its value at a constant level. The comparator makes the decision by comparing the sampled signal (V_{in}) with reference thresholds (V_{ref}) generated by the DAC. The SAR logic stores the digital outputs and reconfigures the DAC to update V_{ref} based on the comparator decision. Since a DAC is composed of many capacitors, it is also called "capacitive DAC" or "CDAC". The top plate of each capacitor is tied to the reference voltage node while the bottom plate can be connected to either supply voltage (V_{DD}) or the ground. The conversion of SAR ADCs proceeds as follows. The Track/Hold circuit samples the analog input during the sampling period. When the ADC steps into the quantization period, the comparator is activated and compares the analog input (V_{in}) with the first reference threshold (V_{ref}). Then the SAR logic yields the MSB output based on the comparison result. In addition, capacitors in the DAC are either charged or discharged to generate a new reference threshold. After the comparator is reset, the next comparison will start and the analog input is compared

with the updated reference threshold. Repetitively, the reference threshold is updated and compared with the input until all digital bits are resolved.

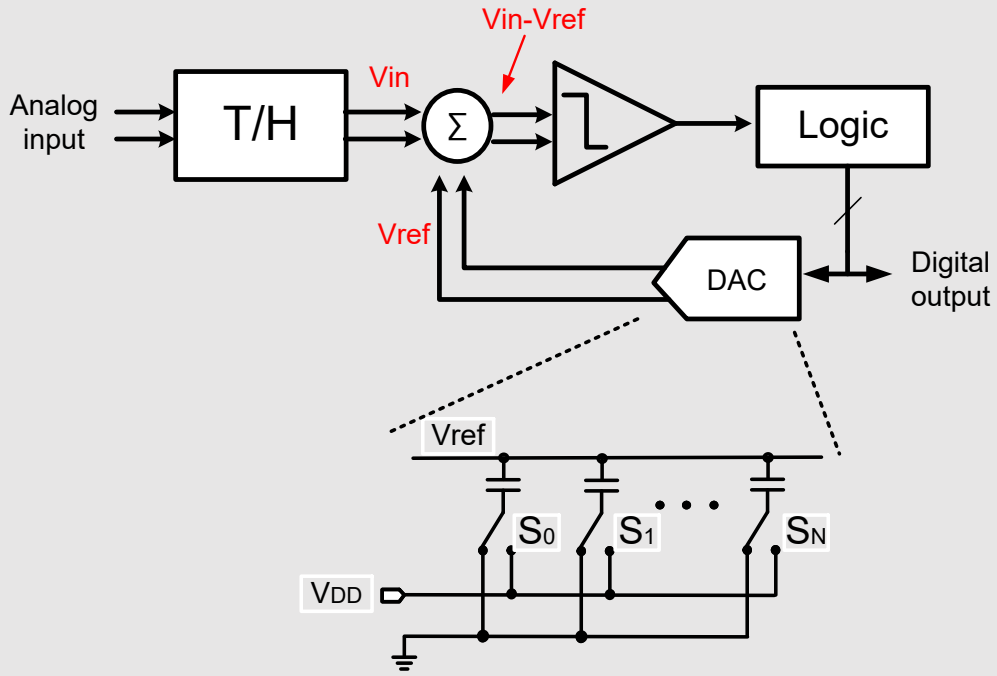

Figure 2.11 SAR ADC diagram

The timing diagram of SAR ADCs is shown in Figure 2.12. A clock period is divided into sampling phase and quantization phase, which is composed of multiple conversion stages. During each conversion stage, one digital bit output is yielded. Since the analog signal is processed in a loop formed by a comparator, a SAR logic and a DAC, the propagation delay of the three blocks all contribute to the period of a conversion stage. However, because the SAR logic only consists of digital gates, its delay is ignorable especially in scaled technologies. As a result, the period of a conversion stage mainly incorporates the comparator resolving time, reset time and the settling time of capacitors.

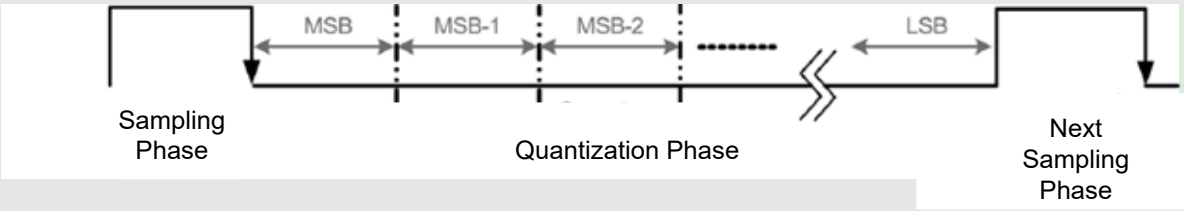

Figure 2.12 SAR ADC timing diagram

Due to the use of one comparator, the power consumption of SAR ADCs is the lowest compared to the other two architectures, but the speed of SAR ADC is less competitive because of the fact that it needs multiple cycles to finish the conversion. According to the survey summarized by Dr.Murmann [5], most SAR ADCs are working at the range of Mega samples per second (MS/s), while flash ADCs can achieve over 1 Giga samples per second (GS/s). However, SAR ADC has attained more favor in recent years since the speed limitation can be overcome by using time-interleaving technique, which allows multiple identical ADCs to process analog signals at a higher frequency. As shown in Figure 2.13, M ADCs operating at sampling frequency of $f_s/_M$ are interleaved together. Since they are working in a sequence and each ADC samples the analog input at different times, the sampling frequency of the entire system can achieve f_s.

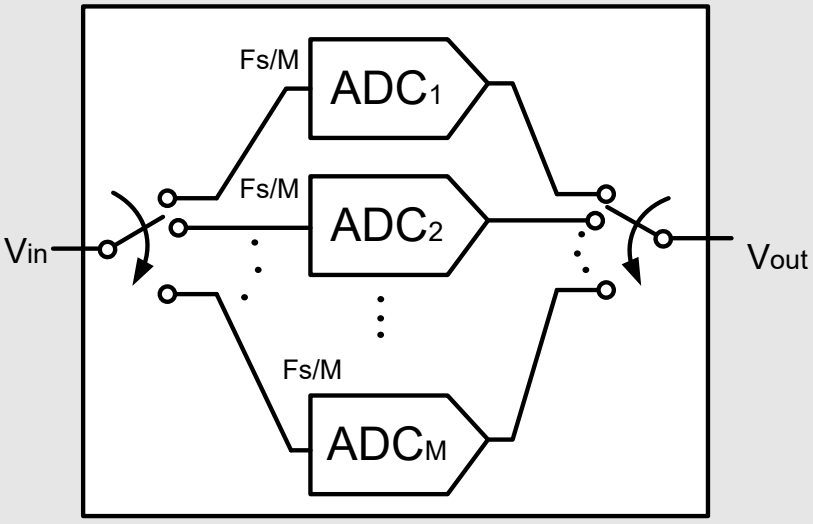

Figure 2.13 time-interleaving ADC structure

2.2.4 Summary

Flash ADCs are attractive in the aspect of speed because all comparisons are done simultaneously. However, $2^N - 1$ comparators are needed to operate simultaneously during quantization, so the main drawback is the exponentially increased power consumption as the number of bit goes up. The 8-bit ADC in this thesis does not adopt this structure due to the cost of high power. Pipeline ADCs can achieve high speed while consuming less power than flash ADCs. Nonetheless, the precise amplification in each stage is hard to be satisfied in scaled technologies, resulting in linearity degraded. In this design, the structure of SAR ADC is used because it is free of amplification and costs extremely low power. In addition, the extensive implementation of digital building blocks makes it compatible with scaled technologies. Even though the conversion speed is not competitive compared to other two architectures, the use of time-interleaving technique can push it to achieve gigahertz of sampling rate, which meets the requirements of many high-speed applications.

Chapter 3

Proposed SAR ADC

In this chapter, the proposed SAR ADC architecture is disclosed. Compared with a conventional structure, two main improvements are discussed which enable the proposed SAR ADC to achieve higher conversion speed.

3.1 Conventional SAR ADC

A conventional SAR ADC using single comparator is described in [1], and its block diagram is shown in Figure 3.1. An SR latch is used to store the comparison result. In addition, the comparison output is detected by a ready generator to generate a ready signal, driving a sequencer to provide multi-phase clocks for bit caches to store the internal comparison result from the SR latch. Simultaneously, the capacitors in the DAC are reconfigured by the switch logic. Furthermore, a separate pulse generator is used to reset the comparator once the ready signal is generated. In [1], a 6-bit SAR ADC is implemented in 0.13μm CMOS technology. It achieves an SNDR of 34dB at 300 MS/s while consuming 5.3mW.

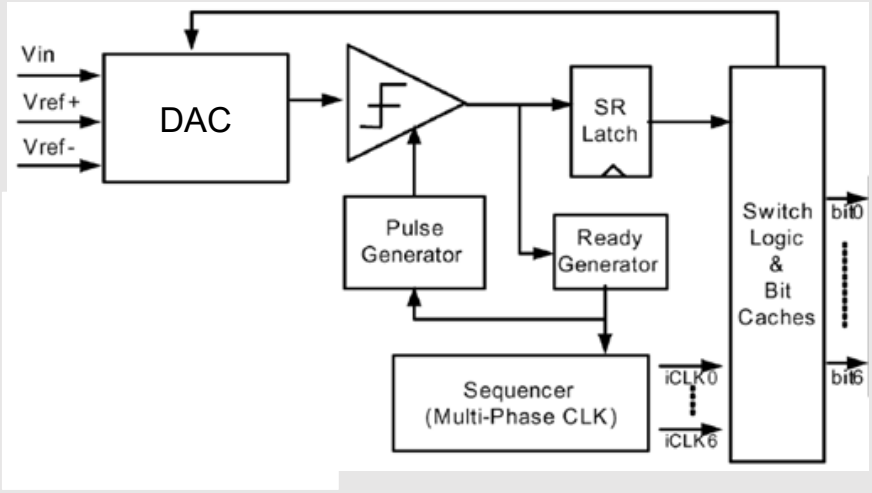

Figure 3.1 A conventional SAR ADC architecture

Two drawbacks exist in the above architecture. First, the single comparator needs to be reset after each decision to avoid any memory effect for the next comparison. For an 8-bit SAR ADC, the comparator is required to be reset 7 times, which slows down the conversion. Second, the single comparator output is used to reconfigure different sets of capacitors in the DAC, so a DEMUX is always contained in the switch logic, which complicates the digital logic design. However, the above two problems are solved in the proposed SAR ADC structure.

3.2 Proposed SAR ADC

Different from the conventional SAR ADC, multiple concurrent comparators are utilized in the proposed structure, as shown in Figure 3.2. Because each comparator is used for only one decision, the memory effect of the previous comparator will not pass to the subsequent one, thus comparisons are activated before previous comparators are reset completely. As a result, the SAR ADC conversion speed is improved. Furthermore, another benefit of using multiple concurrent comparators is that the DEMUX can be removed from the switch logic because each comparator output is used to reconfigure only one set of capacitors in the DAC. Consequently, the digital design is simplified. An 8-bit SAR ADC using multiple concurrent comparators is designed in 65nm CMOS technology. It can achieve an SNDR of 44 dB at sampling frequency of 400 MS/s, which is higher than the conventional SAR ADC in [1].

In the proposed SAR ADC, each comparator is connected to its own digital block (SAR logic), whose responsibilities can be divided into four parts. First, it receives the comparasion decision and outputs the digital code. Second, each SAR logic reconfigures the corresponding set of capacitors to generate a new reference threshold. Moreover, the subsequent comparsion is triggerred by the SAR logic after the current comparison is finished. Finally, the SAR logic resets the current comparator but this process will not delay the entire conversion.

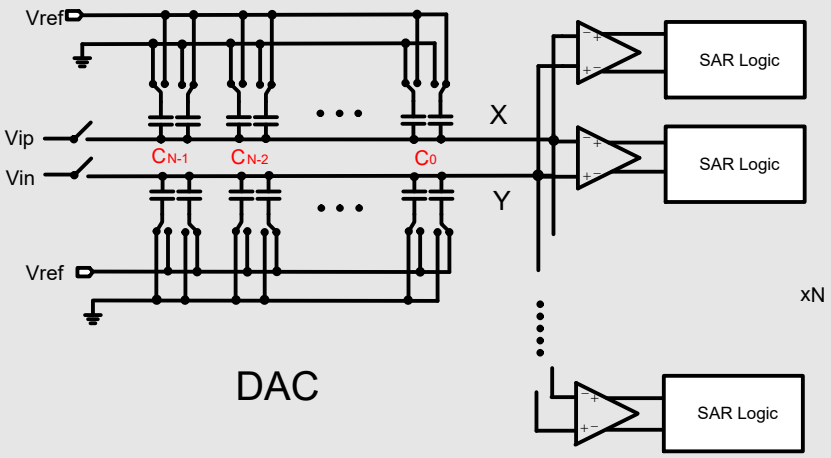

Figure 3.2 Proposed SAR ADC architecture

For an N-bit SAR ADC, the DAC includes N sets of capacitors. Each set is composed of four identical capacitors. Two of them are connected to the node X while the other two are tied to the node Y. The capacitor in different sets are binary-weighted ($C_{N-1} = 2 \times C_{N-2}$). The conversion procedure is illustrated as follows.

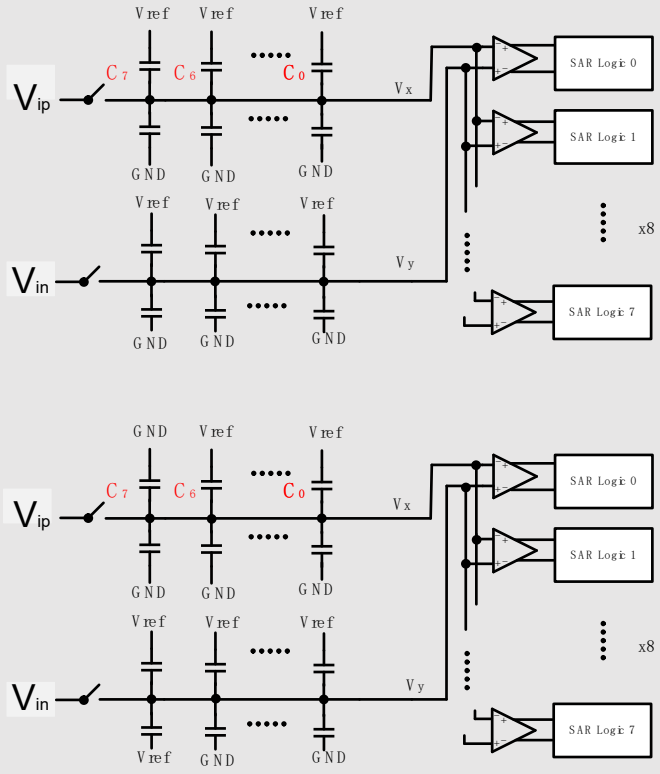

Figure 3.3 Charge redistribution operation (a), (b)

During the sampling phase (Figure 3.3 (a)), half of the capacitors are connected to the supply voltage (V_{ref}) and the other half are tied to the ground. Track/Hold circuits are disengaged from the DAC once differential signals are sampled onto the capacitors. The charge stored in the upper half of capacitors (Q_x) and the charge stored in the lower half of capacitors (Q_y) are derived:

$$Q_x = Q_y = (V_x - V_{ref})C_{tot} + (V_x - 0)C_{tot} = (V_y - V_{ref})C_{tot} + (V_y - 0)C_{tot}$$

Where $C_{tot} = \sum_{i=0}^{7} C_i$. The first comparator directly compares V_x with V_y, which is equivalent to comparing (V_{ip}-V_{in}) with 0 (the middle reference threshold of the searching range). Let us assume $V_{ip} > V_{in}$, then Figure 3.3 (b) shows the first DAC configuration. One capacitor in the first stage that was connected to V_{ref} is switched to the ground; Simultaneously, the capacitor in the first stage on the downside is switched to V_{ref}. The charge stored in the capacitors at this moment can be expressed:

$$Q_x = (V_x' - 0)(C_{tot} - C_7) + (V_x' - V_{ref})(C_{tot} - C_7)$$

$$Q_y = (V_y' - V_{ref})(C_{tot} - C_7) + (V_y' - 0)(C_{tot} - C_7)$$

Because the charge stored in the capacitors is constant before and after DAC reconfiguration, the voltage at node x and node y are updated as

$$V_x' = V_x - \frac{1}{4}V_{ref}$$

$$V_y' = V_y + \frac{1}{4}V_{ref}$$

Then the second comparator compares V_x' and V_y', which is the same as comparing ($V_{ip} - V_{in}$) with $\frac{1}{2}V_{ref}$. If $V_x' > V_y'$. The second stage of DAC acts identically as the first stage to decrease V_x' by extra $\frac{1}{8}V_{ref}$ and increase V_y' by $\frac{1}{8}V_{ref}$. Otherwise, V_x' is raised and V_y' is reduced. After N iterations,

($V_{ip} - V_{in}$) approaches to 0 and N bits are resolved. Note that for differential-input ADC, it is always ($V_{ip} - V_{in}$) compared with different reference thresholds.

Chapter 4

Design Considerations and Simulation Results

In this chapter, the details of each ADC block are disclosed in the aspect of the realization of binary search mechanism. Additionally, the design challenges and considerations of how to overcome them are also discussed. In the end, simulation results and analysis are shown.

4.1 T/H circuit

T/H circuit samples the analog signal onto a capacitor C_s, which stores the value during the quantization. In reality, the sampling switch can be implemented by a MOS transistor and its gate is controlled by the sampling clock CLK, as depicted in Figure 4.1.

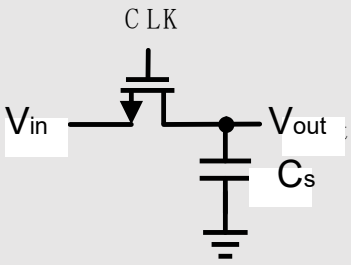

Figure 4.1 T/H circuit model

Figure 4.2 (a) shows the relationship among V_{in}, Vout and CLK. In this example, an NMOS transistor is used. When CLK is logic high (track mode) the sampling capacitor C_s is being charged and the node V_{out} follows the analog input V_{in}. When clock is logic low (hold mode), V_{in} is cut off from V_{out}. The analog sample is kept steady during quantization.

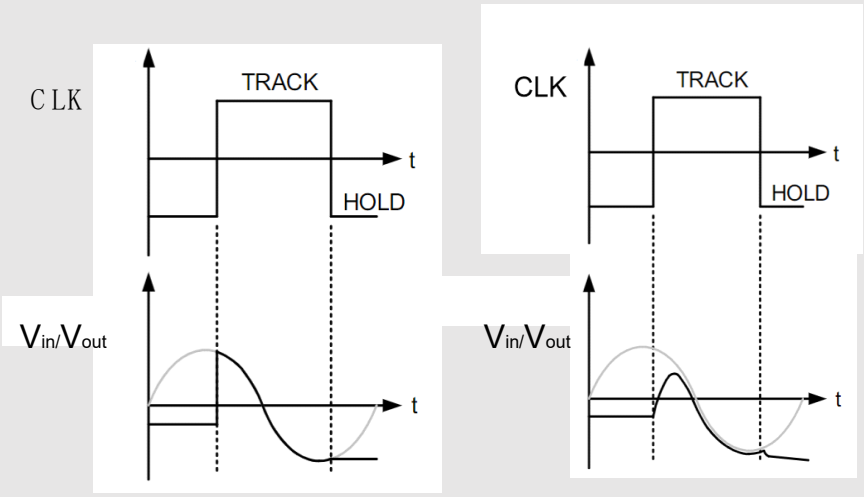

Figure 4.2 Clock, input and output of T/H (a), (b)

However, nonidealities existing in T/H result in the curve of V_{out} that is less ideal as indicated in Figure 4.2 (b). The degraded sampled signal is caused by many sources, which are described in the following sections.

4.1.1 Thermal noise

During the sampling phase when the MOS transistor is conducting, the finite resistance exhibited between source and drain introduces thermal noise. The noise power per unit bandwidth could be derived as:

$$\overline{V_n^2} = 4kTR$$

where k=1.38 × $10^{-23} J/K$ is Boltzmann constant, T=300K is the temperature, and R is the equivalent resistor of the transistor. The total noise power is the integration of $\overline{V_n^2}$ over frequency. Since the RC network is a low-pass filter, the noise power at the sampler output is:

$$P_{n,out} = \int_0^\infty \frac{4kTR}{4\pi^2 R^2 C^2 f^2 + 1} df = \frac{kT}{C}$$

Therefore, thermal noise, determined by temperature and sampling capacitance, would deteriorate the sampled signal. Note that the thermal noise at the output of the T/H circuit is independent of transistor resistance R.

In the SAR structure, explicit sampling capacitor is not necessary in that the DAC is directly tied to the T/H circuit and can act as the sampling capacitor. In order to diminish the thermal noise, the comparatively large capacitance of DAC is chosen to make thermal noise smaller than the quantization noise, which is still the dominant noise source.

$$\frac{1.38 \times 10^{-23} \times 300}{256C_u} < \frac{LSB^2}{12}$$

$$C_u > 0.053 \text{ fF}$$

The total capacitance is $256C_u$ on each input side, and $\frac{LSB^2}{12}$ is quantization noise power. 0.4 fF of unit capacitance is chosen so to make the quantization noise greater than the thermal noise.

4.1.2 Tracking nonlinearity

As depicted in Figure 3.1, the T/H circuit is a RC network if we assume that the equivalent resistance of the sampling transistor is stable. Then the time response is derived as:

$$V_{(t)} = V_0 + (V_u - V_0)(1 - e^{-\frac{t}{RC}})$$

where V_0 is the initial voltage at the output and V_u is the input voltage or the ultimate value the capacitor is charged up to. The difference between the sampled value and the analog input is defined as the charging error. The more time allocated for the sampling period, the smaller the charging error would be. Enough sampling time should be assigned in the worst sampling case, which happens when ADC samples the lowest input in the previous cycle and the highest input in the next cycle, as shown in Figure 4.3, because the voltage change at the output of the sampling circuit spans over full-scale range.

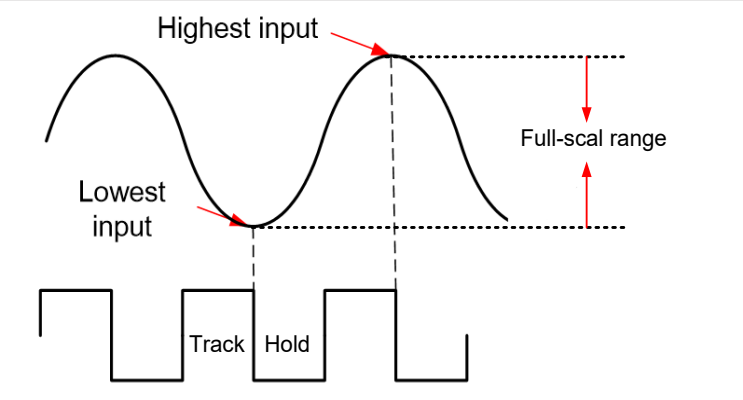

Figure 4.3 Worst case when sampling the input signal

The charging error then is formulated as

$$Error = V_{FS}e^{-\frac{mTs}{RC}}$$

where V_{FS} is the full-scale range of input signal and mT_s is the sampling time. The error should be less than the quantization error so the degraded sample would not affect the resolution of entire ADC.

However, the equivalent resistance of transistor is not constant during sampling and it is dependent on input signal:

$$R_{on,NMOS} = \frac{1}{\mu Cox\frac{W}{L}(V_{GS} - Vth)} = \frac{1}{\mu Cox\frac{W}{L}(VDD - Vin - Vth)}$$

The equivalent resistance depends on the voltage between the gate and the source. If taking NMOS as the sampling switch, the gate is always connected to V_{DD} and the source is tied to the input. When V_{in} sweeps to the highest level, R_{on} becomes greater compared to the case when V_{in} reaches the lowest level. Variable R_{on} causes nonlinear sampling circuits, resulting in degraded resolution. The signal being sampled is shown in Figure 4.4.

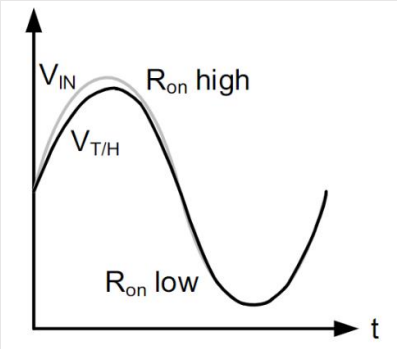

Figure 4.4 Equivalent resistance of sampling NMOS

The solution to this problem is implementing the CMOS transmission gate as the sampling switch shown in Figure 4.5. When V_{in} is close to V_{DD}, R_{on} of NMOS is extremely high, while large V_{SG} makes PMOS exhibit low R_{on} so the sampling circuit can still track the input well. Oppositely, when V_{in} reaches the lowest level, NMOS representing low R_{on}would let the signal through.

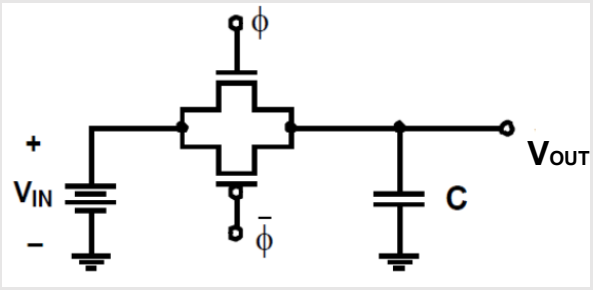

Figure 4.5 CMOS transistor as sampling switch

The equivalent resistance of CMOS switch is independent of input $if\ \mu_n[\frac{W}{L}]_n = \mu_p[\frac{W}{L}]_p$, as shown in the deductions("||" denotes that two terms are in parallel):

$$R = \frac{1}{\mu_n Cox[\frac{W}{L}]_n(V_{GSn} - Vthn)} \| \frac{1}{\mu_p Cox[\frac{W}{L}]_p(|V_{GS}| - |Vthp|)}$$

$$= \frac{1}{\mu_n Cox[\frac{W}{L}]_n(V_{DD} - Vin - Vthn)} \| \frac{1}{\mu_p Cox[\frac{W}{L}]_p(Vin - |Vthp|)}$$

$$= \frac{1}{\mu_n Cox[\frac{W}{L}]_n(V_{DD} - Vthn - |Vthp|)}$$

In the real design, it is difficult to size the transmission gate so to meet $\mu_n[\frac{W}{L}]_n = \mu_p[\frac{W}{L}]_p$. But the linearity that the CMOS T/H circuit provides should be enough for ADCs with resolution less than 8 bits.

4.1.3 Charge injection

During sampling, the electrons are accumulated in the transistor channel and those electrons cannot spread instantaneously, so the charge flows into the source and the drain during quantization. As a result, the potential of the real output has a voltage droop when it enters the hold mode (Figure 4.6).

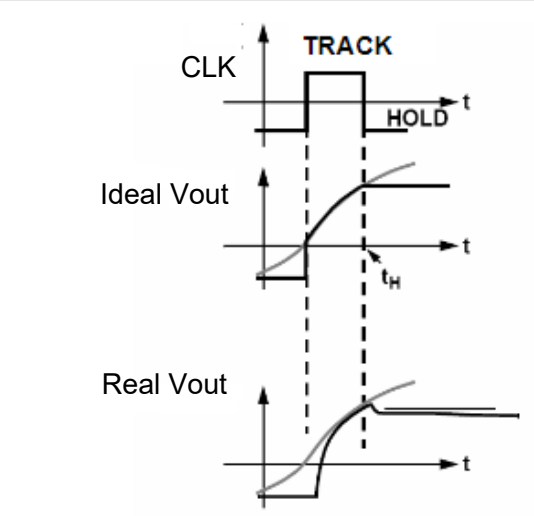

Figure 4.6 sampled signal influenced by charge injection

This problem can be alleviated by using the dummy transistor shown in the Figure 4.7 [5]. M_2 is the same transistor as M_1 but the drain and the source are shorted and the width is reduced by half. When the charge of M_1 flows to the output node after sampling, the same amount of charge is drawn to the channel of M_2, leaving the output potential unchanged. This can be achieved by using two opposite clocks for M_1 and M_2.

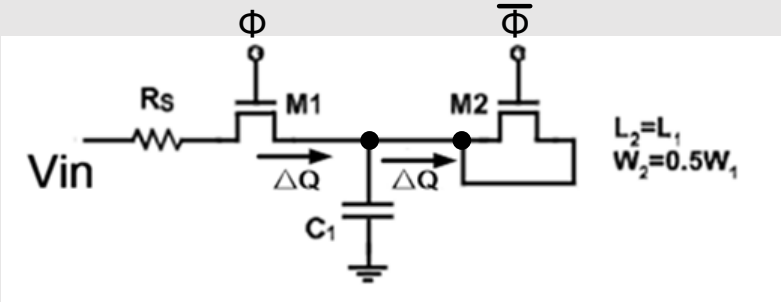

Figure 4.7 Sampling circuit with dummy switch

4.1.4 Input feedthrough

During quantization, the sampled value should be kept steady, but the input signal is coupled to the output through parasitic capacitors as depicted in Figure 4.8, thus deteriorating the sampled signal.

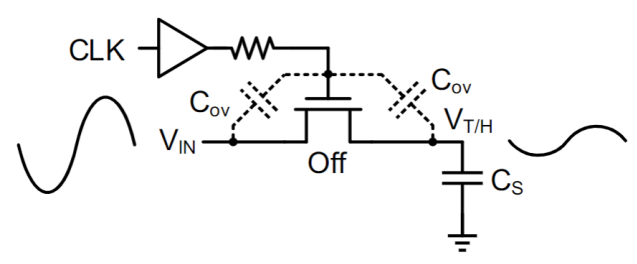

Figure 4.8 Parasitic capacitors causing signal feedthrough

The solution is using extra transistors, as shown in Figure 4.9, to cancel unwanted signals. Transmission gates T_1 and T_4 are sampling switches while T_2 and T_3, always being off, are used to cancel the signal feedthrough. During hold mode, for an instance, VINP would be coupled to OUTP through T_1 and VINN would also be coupled to OUTP. Because VINP and VINN are differential signals, the coupling effects are cancelled out at the output node.

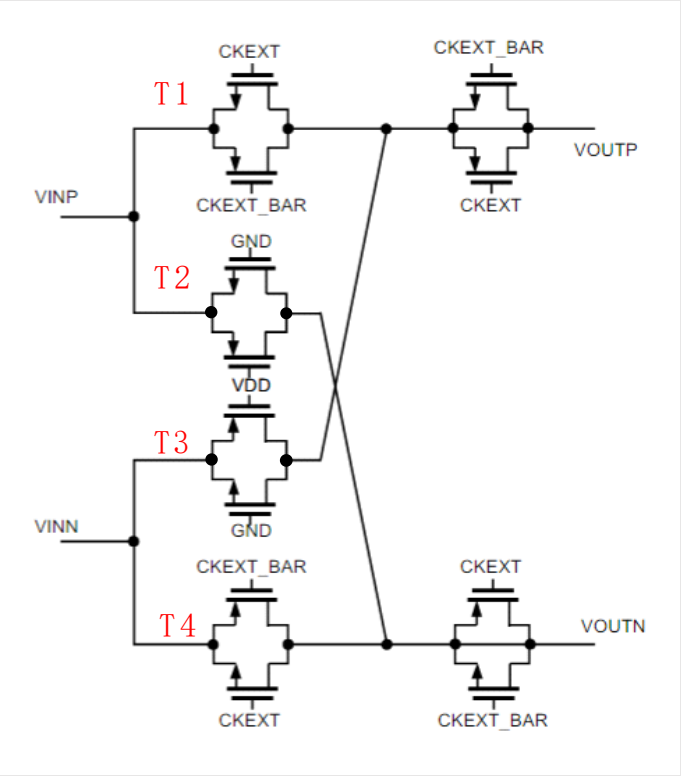

Figure 4.9 Cross-coupled T/H with dummy switch

4.1.5 Bootstrapped T/H Circuit

For the ADC of high resolution, the bootstrapped T/H circuit is always used, which has better linearity than the CMOS counterpart. The idea is to lock V_{GS} of the sampling switch and the equivalent resistance is stable no matter how the input varies.

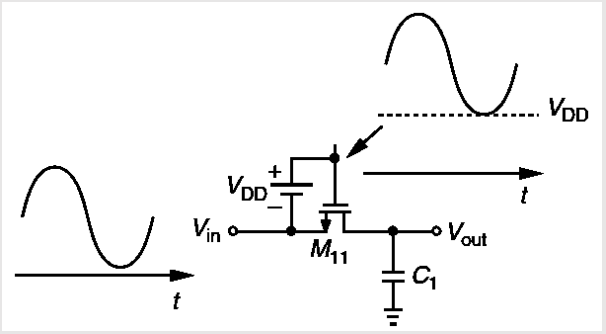

Figure 4.10 T/H boosted by battery

The bootstrapped T/H is modeled in Figure 4.10. A battery put in the circuit makes the gate potential change with the source potential at the same pace, so to provide the switch with a constant V_{GS}.

The Figure 4.11 describes the simplified implementation of bootstrapped T/H where the battery is replaced by a pre-charged capacitor C_b. In the hold mode, switch M_{10} is open so Vout is disengaged from V_{in}; M_8 and M_9 are open while M_3 and M_{12} are closed to charge C_b to V_{DD}. In the sampling mode, the status of all switches is inverted so the capacitor is connected between the gate and the source to lock V_{GS}.

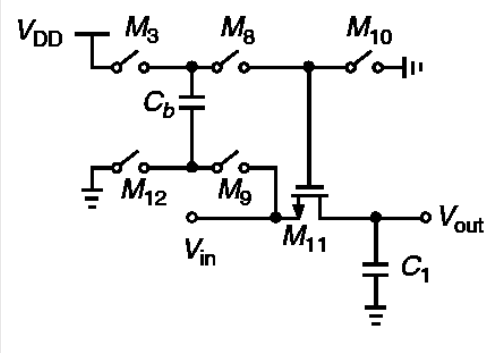

Figure 4.11 Simple bootstrapped T/H structure

The completed bootstrapped T/H circuit [12] is shown in Figure 4.12. The circuit enters the hold mode when CK falls to logic 0 and $\overline{CK}$ rises to logic 1. In the hold mode, M_{11} is connected to ground through M_{14} and M_{10}; M_3 and M_{12} are turned on to charge C_b to V_{DD}. In the sampling mode, $M_8$and M_9 are turned on to form a loop so the precharged capacitor locks V_{GS} constantly. The gate of M_3 cannot be tied to CK directly because the potential of node P might exceed V_{DD} by more than V_{thp}, resulting the source and the drain of M_3 exchange their roles and M_3 will be turned on mistakenly. Therefore M_3 is always off during sampling by connecting the gate to the node X. If without M_{14}, V_{GS} and V_{DS} of M_{10} are greater than V_{DD}, resulting in shortened device lifetime and must be avoided. The cascaded structure composed of M_{10} and M_{14} limits V_{GS10} and V_{DS10} to about $V_{\mathrm{DD}}-V_{th14}$, maintaining the circuit for long-time use.

Bootstrapped T/H circuits can provide high linearity at the cost of adding extra transistors and the structure discussed above has been used in a lot of high-speed ADCs with resolution from 8 bits to 12 bits. [13]

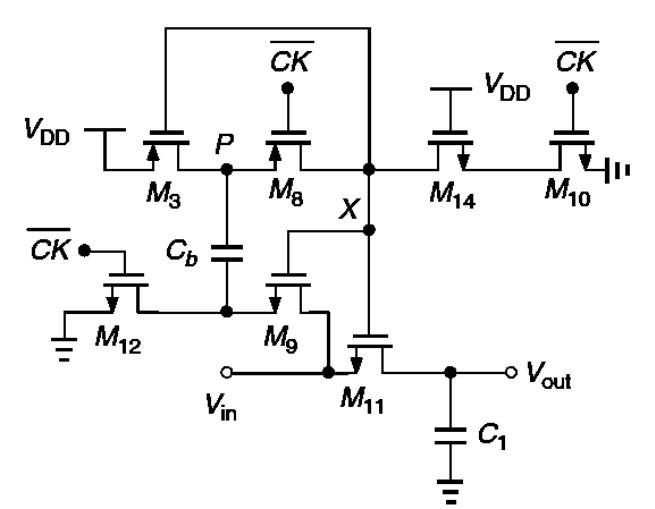

Figure 4.12 Complete bootstrapped T/H structure

4.1.6 Summary

Several nonlinearities that result in degraded sampled signal as well as improvements are introduced above. In this design, the CMOS T/H circuit is implemented to provide high linearity and the dummy switch is used to reduce the charge injection. In addition, the unit capacitor in the DAC is chosen comparatively large so the effect of thermal noise is declined.

4.2 Dynamic regenerative comparator

One of the most important steps in Analog-to-Digital conversion is comparing the analog input with different threshold references to generate digital codes, so the comparator is a necessary block used in all commonly used ADCs. For recent years, the need for highly integrable and programmable ADCs are pushing towards the use of dynamic regenerative comparators, which bring huge advantages over static comparators that suffer from high power consumption and limited speed [10].

4.2.1 Comparator structure

As shown in the Figure 4.13, the comparator contains two stages: preamplifier and dynamic latch. The cross-coupled inverters (M_{11}, M_{14} and M_{14}, M_{15}) in the latch use a positive feedback mechanism to regenerate the analog input signal into a full-scale digital level. The operation is as follows:

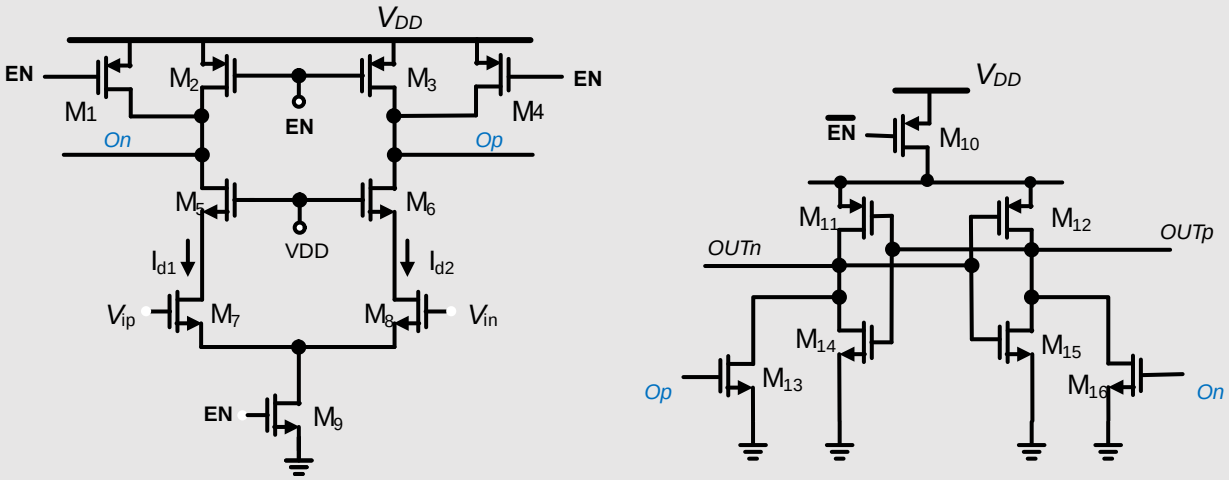

Figure 4.13 Comparator architecture

During reset phase (when EN=0), M_3 and M_{10} are off so there is no current drawn from supply voltage, and M_1-M_4 pull intermediate nodes O_{n} and O_{p} to V_{DD} while M_{13} and M_{16} pull the output nodes OUT_{n} and OUT_{p} to the ground, defining a start condition. The input voltages to be compared are applied to nodes V_{ip} and V_{in}. In the comparison phase (when EN=1), M_1-M_4 are off while M_9 is conducting so the voltages of intermediate nodes are decreasing; M_{10} is conducting to charge OUT_{p} and OUT_{n}. For the case where V_{ip}> V_{in}, the voltage of O_{n} is dropping faster than O_{p}. The entire cross-coupled inverters initiate regeneration when O_{n} is discharged to V_{thN} before O_{p} reaches the same voltage level. Then OUT_{p} would be pulled up the V_{DD} through $M_{11}$and M_{10}while OUT_{n} is discharged to the ground through M15. During the Process, V_{DD} only supplies the current at the beginning of the reset phase and the comparison phase. It is more power efficient compared to static comparator used in [8].

4.2.2 Preamplifier

The preamplifier is necessary in front of the dynamic latch for at least two reasons: metastability limitation and offset reduction.

Metastability is a problem that occurs in all latching comparators when the value of two inputs are close to each other. Consequently, the comparator would take more time to switch to a valid output state than is available in the comparison period. Since asynchronous ADCs require the comparator to trigger subsequent logics automatically, uncertain delay caused by metastability may stall the entire ADC and the digital output is meaningless. Fortunately, the upcoming sampling cycle would reset comparators and all we lost is the previous data point, but if the probability of this problem occurring is high, the resolution of ADC is degraded.

Applying the preamplifier can help this issue since it amplifies the sampled inputs before they go into the dynamic latch. The gain of preamplifiers is analyzed in [9]. The input signals applied at V_{ip} and V_{in} include common mode signal and differential part. If only considering the differential signal and assume the input is $\frac{\Delta \mathrm{V}}{2}$, the current difference generated at the drain of M_7 and M_8 $(I_{d1} - I_{d2})$ is $G_m \frac{\Delta \mathrm{V}}{2}$, where G_m is the transconductance of M_7 and M_8. The operation of preamplifiers during comparison phase is to discharge intermediate nodes Op and On, which are both precharged to V_{DD} at reset. And the voltage difference with the respect to time is derived:

$$O_P - O_N = [G_{m7} \frac{\Delta \mathrm{V}}{2} - G_{m8}(-\frac{\Delta \mathrm{V}}{2})] \times \frac{t}{C_{load}}$$

The gain of preamplifier with respect to time is $G_{m7,8} \frac{\Delta \mathrm{t}}{C_{load}}$, indicating that the larger size of input pair can provide higher gain, leading to reduced probability of metastability.

The offset problem is always existing in the comparator when the input transistors are not well matched with each other, leading the comparator to yield wrong digital outputs. It happens a lot because mismatch is hard to be avoided in the fabrication especially when two transistors are sized too small.

Using preamplifier can reduce the mismatch effect on the dynamic latch. For example, if the preamplifier gain is 10 and the input-referred offset of dynamic latch and preamplifier due to mismatch are 30mV and 3mV, then the input-referred offset of entire comparator is $\sqrt{(3mV)^2 + \frac{1}{10}(30mV)^2} = 4.2mV$.

4.2.3 Power consumption analysis of the dynamic latch

The comparator is a main part in the entire ADC power budget, especially for the ADC of this design where 8 comparators are used for speed enhancement, so it is crucial to achieve a balance between comparator delay and power when sizing the transistors. [8] analyzes the power of the dynamic latch and shows the trade-off between the speed and power. It uses a time-variant model which emulates the operation of transistors during the dynamic operation in comparison phase.

Theoretically, the power of supply voltage during one period of comparison is obtained from:

$$Power_{avg} = \frac{1}{T}\int_0^T V_{DD} I_{supply} d_t = f_{clk} V_{DD} \int_0^T I_{supply} d_t$$

During a short period of time in the dynamic operation of comparison phase, a current is drawn from V_{DD} to the drain of PMOS transistors M_{11} and M_{12}. If we plug the single expression for drain current into the formula, the closed-form expression for the dynamic latch power consumption is derived as below:

$$Power_{avg} = f_{clk} V_{DD} I_{SP} \left(\frac{1}{8n\varphi_t^2}\right) \tau_{latch} |V_{thp}| \times [2k - n]|V_{thp}| + (2k + n)|V_{thp}| \times$$

$$\exp\left(-2\frac{t_p - t_0}{\tau_{latch}}\right) - 4\mathrm{k} \times \exp(-\frac{t_p - t_0}{\tau_{latch}})$$

in this equation, k is equal to $V_{DD} - |V_{thp}|$; $t_p - t_0$ are the time period used for regeneration. I_{sp} is positive related to the size of M_{11} and M_{12}. τ_{latch} is positive proportional to the effective transconductance of the PMOS and NMOS transistors in the regenerative latch.

The equation indicates that the most influential design parameters for the power consumption are clock frequency, size of dynamic latch transistors, supply voltage and the comparison time. And the intuition that it provides is helpful when designing the comparator. For an instance, in order to reduce the power consumption, smaller size of PMOS is chosen so I_{sp} is reduced. But Gm of the latch inverter is also decreased with smaller W/L, leading to larger comparison time $t_p - t_0$.

4.2.4 Comparator Background Calibration

As discussed in Section 3.2.2, mismatches in comparators between differential inputs bring about offset, which have been regarded as an uncontrolled parameter that has great limitation on ADC resolution. Even though the offset originates from the process non-uniformity, there are many calibration methods to eliminate it at the circuit level.

Foreground calibration is a method to remove the offset at a dedicated time interval during which the ADC are stalled. In this way, since ADCs are typically calibrated once before they start working, the offset is changeable due to PVT variations, thus the linearity will still be degraded in cases where temperature and supply voltages are inconstant.

On the contrary, the background calibration tracks the PVT variations and it adjusts the comparator offset continuously without interrupting ADC's normal operation. [11] describes a background calibration method that does not need extra clock phase and the circuit overhead is small.

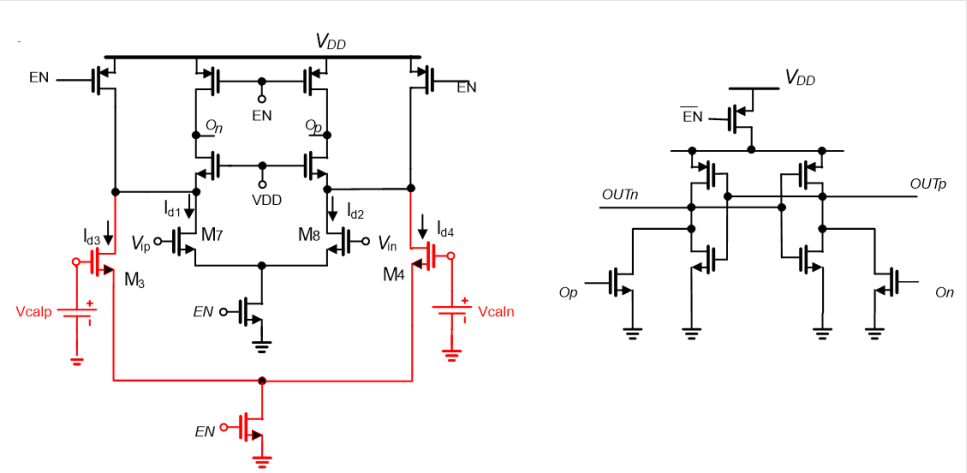

Figure 4.14 Comparator with voltage source calibration

Figure 4.14 shows the basic idea of comparator calibration where two extra voltage sources $V_{\mathrm{calp}}, V_{\mathrm{caln}}$ and two redundant input transistors M_3, M_4 are added. Assume all offsets are referred to the input pair M_7 and M_8. Ideally, the currents flowing into the drain of input pair M_7, M_8 are equal if input voltages V_{ip} and V_{in} are identical (I_{d1}=I_{d2}), but due to mismatched M_7 and M_8, O_{n} and O_{p} are discharged at different rate, leading the comparator to give a wrong output. Fortunately, by calibration method, the added pair M_3 and M_4 are controlled purposely by voltage sources and generates calibrated current to compensate the unmatched currents (I_{d1}+I_{d3}=I_{d2}+I_{d4}), resulting in $O_{\mathrm{p}}$and O_{n} discharged at even speed.

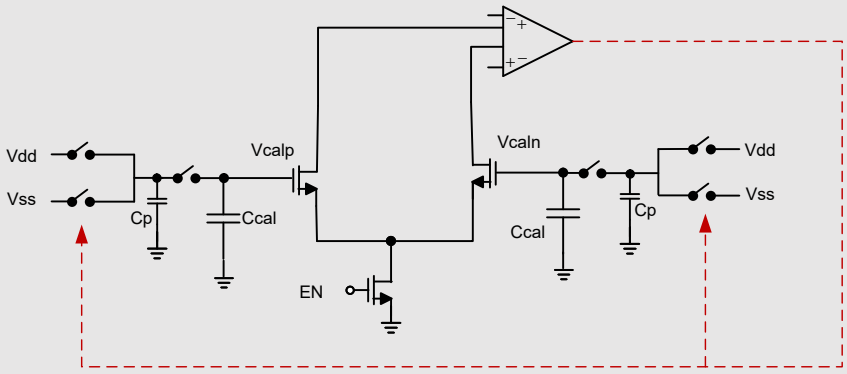

Figure 4.15 Diagram of background calibration

Figure 4.15 elaborates the calibration achieved in background. Large capacitors C_{cal} act as voltage source, being charged or discharged to adjust the calibrated voltages. The small capacitors C_{p} are used to share the charge with C_{cal}. At the beginning, the comparator is activated with shorted inputs so its output reflects the offset information, which is used to determine whether C_{p} is charged to V_{DD} or discharged to ground. Then, C_{p} is disengaged from V_{DD} or the ground and connected to C_{cal} to share the charge. Since $C_{\mathrm{p}} << C_{\mathrm{cal}}$, the calibration voltages V_{calp} and V_{caln} are tuned by small steps.

The completed circuit is shown in Figure 4.16. When Calib=0 and Calib_b=1 the comparator is in the regular mode. C_{p1} is discharged to the ground through M_{11} and C_{p2} is charged to V_{DD} through M_{14}. It enters calibration when Calib=0. Let us assume outP=1 and outN=0 after M15 shorts the inputs.

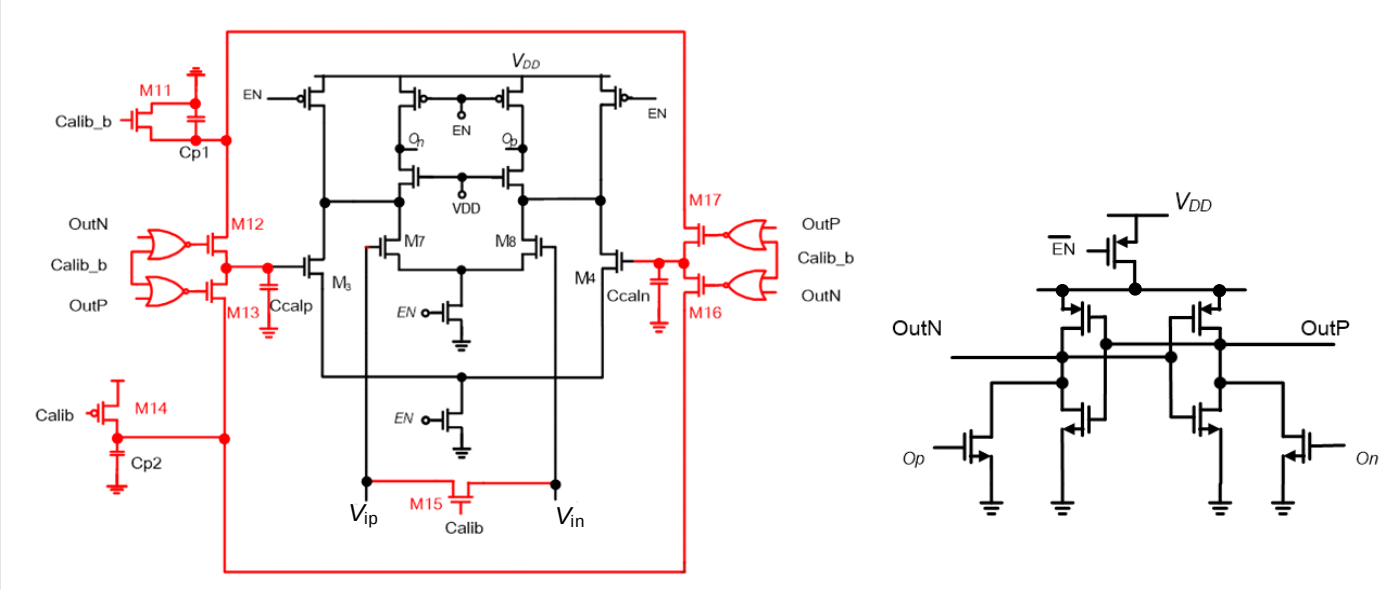

Figure 4.16 Complete structure of background calibration

M12 is conducting so C_{calp} is connected to C_{p1} and V_{calp} is decreased, while M_{16} is turned on so C_{caln} is charged by C_{p2} and V_{caln} is increased. The calibration is executed only one time during every quantization period and the comparator would finally reach the stable state where the output alternates

with ‘1’ and ‘0’ as depicted in Figure 4.17. (The comparator has offset initially so outP is always ‘1’ while outN is ‘0’. The stable state is achieved when two are yielding alternative opposite outputs.)

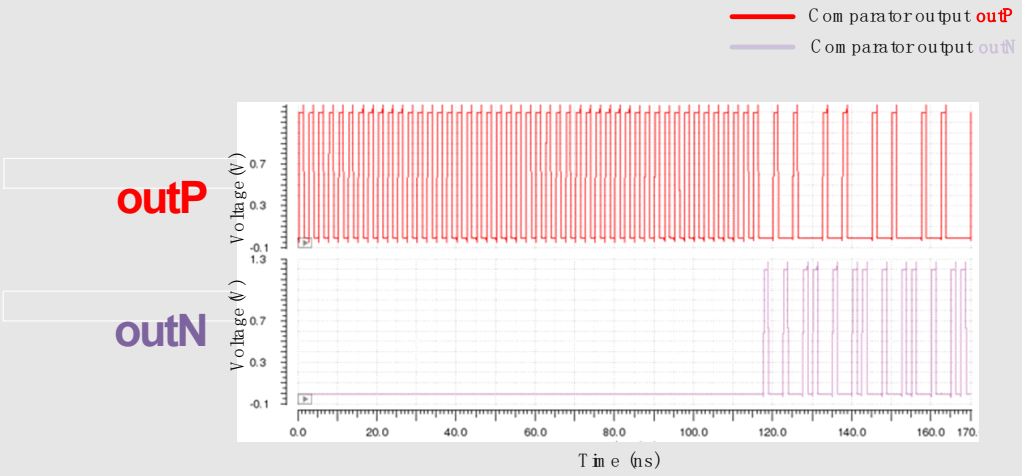

Figure 4.17 Comparator output during calibration

If plotting out the transient curve of V_{calp} and V_{caln} (Figure 4.18), we can find that the two signals are varying at the beginning and will be settled after a period of time.

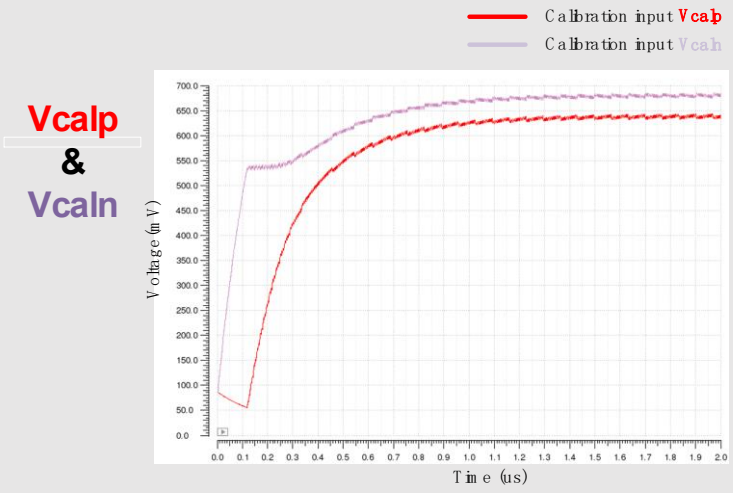

Figure 4.18 Transient curves of V_{calp} and V_{caln}

For the above calibration method, C_{p1} and C_{p2} cannot be extremely small capacitors because it is hard to make precise small capacitors in the fabrication. Thus, in order to achieve a small calibration step, the capacitance of C_{calp} and C_{caln} need to be huge, which enlarge the comparator area. However, the calibration architecture in [12] uses parasitic capacitors of transistors to fine-tune the calibrated voltage and a smaller step of adjustment can be achieved.

In Figure 4.19, SC-Cal is the calibration block enabled by clock en_{cal}, which is connected to every other transistors ($V_{\mathrm{p1-4}}$ and $V_{\mathrm{n1-4}}$) and the comparator output Q_{p} and Q_{n} are tied to others; C_{parp} and C_{parn} are parasitic capacitors of the transistors. The basic idea is same with the previous method that the comparator outputs determine whether to charge or discharge C_{cal}. When en_{cal} is high level, V_{p3}, V_{p1} or V_{n3}, Vn1 are conducting and every parasitic capacitor shares charge with others that is next to itself; When CK_{up} or CK_{dn} are high level, V_{cal} is updated and capacitors at the tail end(C_{parp4} and C_{parn4}) are charged to V_{DD} or discharged to ground;

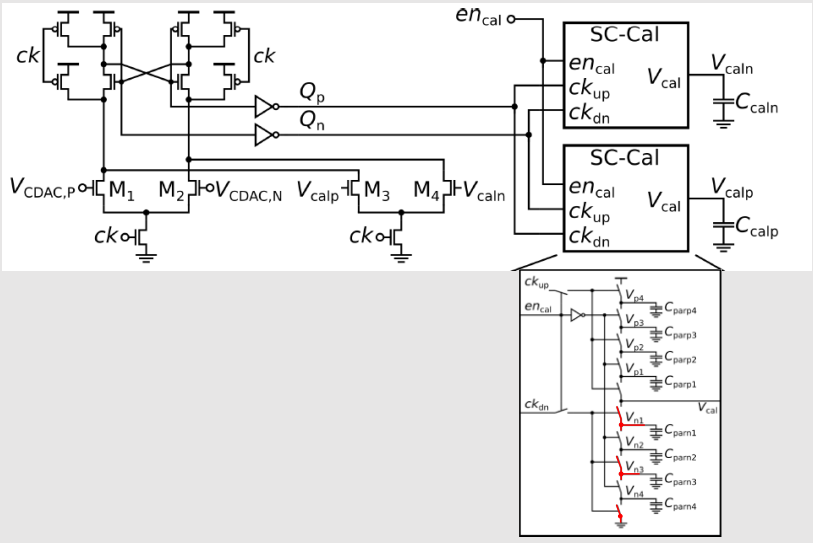

Figure 4.19 Background circuit diagram (method 2), from [15]

By using this structure of calibration, the tuning step is smaller at the cost of the initial time for V_{caln} and V_{calp} to converge to a stable state is longer than the previous method, as shown in Figure 4.20. In the simulation result, the green and yellow curves are V_{calp} and V_{caln} in new structure compared to the previous two counterpart signals. 40 microseconds of time is needed for initiation, which is acceptable in ADC use.

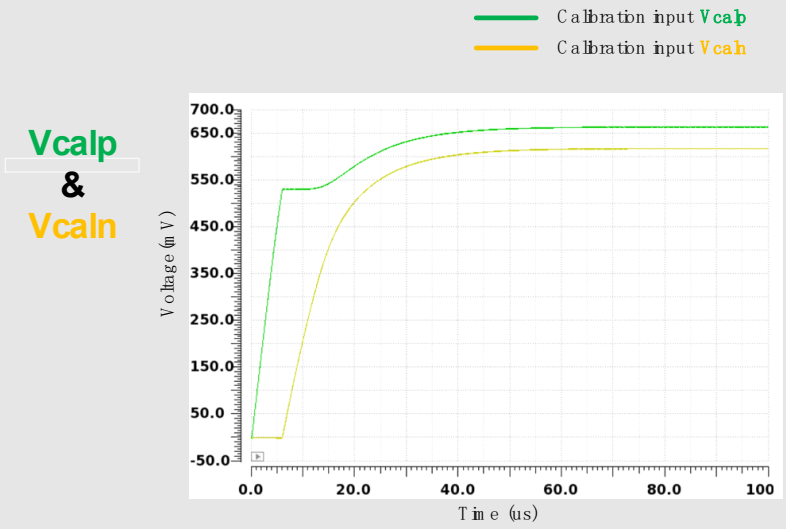

Figure 4.20 Transient curves of V_{calp} and V_{caln} (method 2)

4.3 DAC (Digital-to-Analog block)

Digital-to-Analog blocks are of great importance in ADC operations. The responsibility of the DAC is to receive digital control signals from a SAR logic and use it to update reference voltages for comparators to make decisions. In this section, the DAC structure is elaborated and the energy of the DAC reconfiguration is calculated.

4.3.1 DAC structure

The DAC structure used in this design is shown in Figure 4.21. For 8-bit ADC, 7 stages of DAC are needed and the capacitance of each stage is twice of the previous one. Each stage contains 4

capacitors connected to either V_{ref} or the ground. Analog signals are sampled directly onto summing nodes of the capacitors, so the first comparison can be performed without DAC switching.

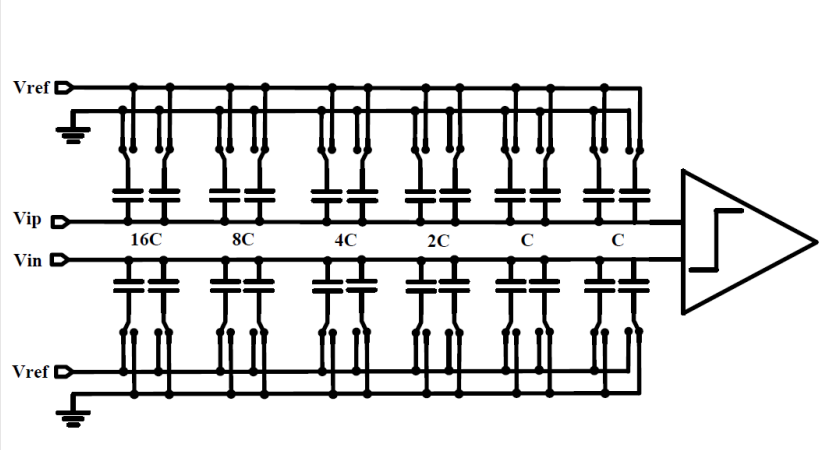

Figure 4.21 8-bit DAC structure

Every time of reconfiguration enables V_{ip} and V_{in} to change in opposite direction by the same amount, which keeps differential inputs a constant common mode voltage. For an instance, V_{ip} is increased by $\frac{1}{4}Vref$ while V_{in} is decreased by $\frac{1}{4}Vref$. As we mentioned in Section 3.2.2, the decision speed of comparators is based on V_{GS} of input differential pair, which is determined by the common mode voltage of the DAC outputs. If V_{cm} keeps decreasing during quantization, comparators may step into metastability condition.

4.3.2 DAC Switching Energy

SAR ADCs are widely used because of their outstanding energy efficiency at moderate speed. DAC switching and comparator are two main contributors to the SAR power budget [9], so the computation of the switching energy is of importance. Figure 4.22(a), (b) shows one DAC switch where the input V_{ip} is increased by $\frac{2}{5}Vref$ after C_1 is reconnected to reference voltage.

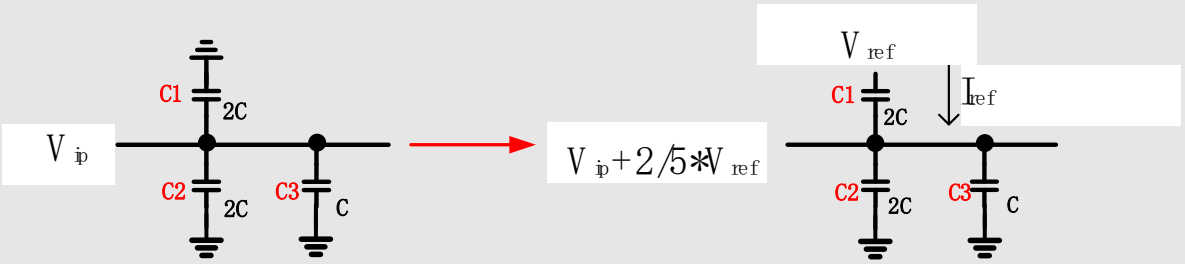

Figure 4.22(a), (b) Switching energy calculation

The dynamic current I_{ref} is flowing from supply voltage into the network and the switching energy can be calculated by the equation:

$$E = \int_0^T Iref(t) * Vref \, dt$$

and the current is derived as:

$$Iref = -\frac{dQc}{dt},$$

Combining two equations:

$$E = -Vref * \int_0^T \frac{dQc}{dt} dt = -\text{Vref} * \int_0^T dQc$$

$$= -Vref * \big(Qc(T) - Qc(0)\big) = -Vref * 2C * \left[\left(Vx + \frac{2}{5} * Vref - Vref\right) - Vx\right] = \frac{6}{5} CVref^2$$

For each DAC switching, there are multiple possibilities and more than one switching energy can be derived. Usually, switching map is drawn and average energy is calculated for each switch so the power efficiency of different types of DAC structures can be compared.

Figure 4.23 shows the energy map of a 3-bit DAC and the average energy that it costs is $4.875CV^2$.

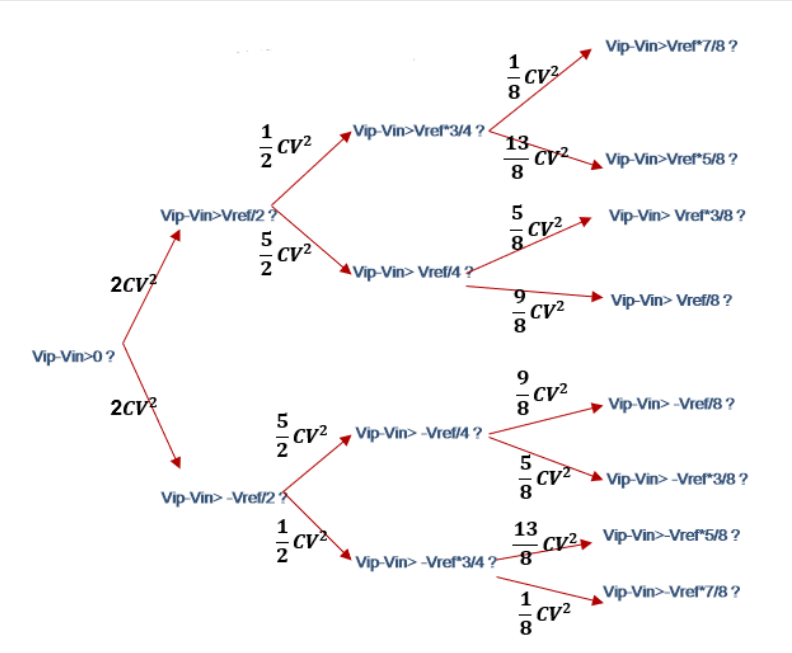

Figure 4.23 Switching energy map of the DAC

4.4 SAR Logic

4.4.1 SAR Logic Operation

Once the comparator gives the decision, the SAR logic stores the digital output and reconfigures the DAC to prepare for next conversion. Moreover, another responsibility of it is to activate next comparison after the DAC is settled, maintaining the proper asynchronous operation. Instead of one SAR logic block which implements all operational controls, eight are used in this design and each of them contributes to only one resolved bit, resulting in much simpler structure.

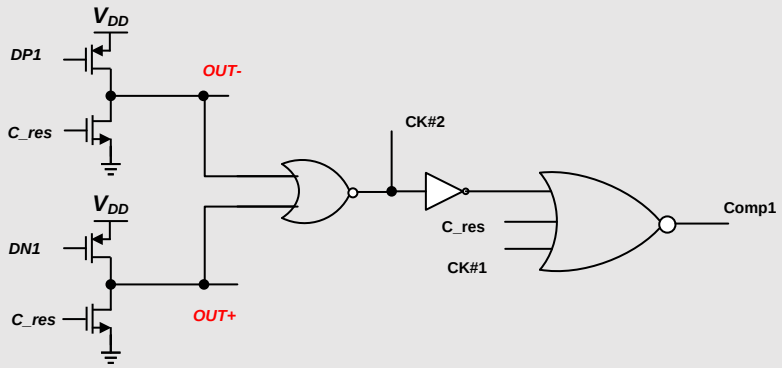

Figure 4.24 SAR logic structure

Figure 4.24 shows the inner structure of a SAR logic block. It is reset by signal $C_{\_res}$ every cycle before sampling; C_{omp1} is the signal to activate or deactivate the comparator, whose differential outputs $DP1$ and $DN1$ are fed to the SAR logic. Since the SAR operation is asynchronous and no extra clock is distributed for turning on each comparator, $CK_{\#1}$ and $CK_{\#2}$ are needed to make the operational connection between previous and subsequent comparators. For example, when it is reset phase and each comparator is off, $C_{\_res}$ rises to pull both outputs down to ground; $DP1$ and $DN1$ are both logic '1' and C_{omp1} =1 at the moment. During quantization when $C_{\_res}$ =0, $CK_{\#1}$ switches from '1' to '0' and C_{omp1} = 1 so the first comparison is triggered. One of $DP1$ and $DN1$ will be set to '0' as the comparator result so $CK_{\#2}$ is set to '1' and C_{omp1} is pulled down to '0', turning the comparator off.

It is worth mentioning that there are three operations after the comparator yielding outputs. First, OUT+ and OUT- are directly connected to the capacitor switches in the DAC, leading to the reconfiguration occurring. Moreover, $CK_{\#2}$ of the current SAR logic is tied to $CK_{\#1}$ of the subsequent one, so the next comparison is triggered right after the previous one. Finally, the comparator is shut off right after its use, so each one only works for a short period and the dynamic power is small.

4.4.2 Connections between SAR logic and DAC

Figure 4.25 elaborates how the DAC is connected with a SAR logic. The outputs of a SAR logic are connected to the DAC capacitors through inverter chains. Because the impedance of internal nodes OUT- and OUT+ is smaller than the capacitance of DAC capacitors, the size of inverters in each connection path needs to be gradually increased so the delay of the capacitor settling is optimized.

During the reset phase, half of capacitors are tied to V_{ref} (from CP/N0+ to CP/N6+) and the other half are connected to ground (from CP/N0- to CP/N6-). During quantization, each stages of capacitors are reconfigured automatically according to the comparator outputs.

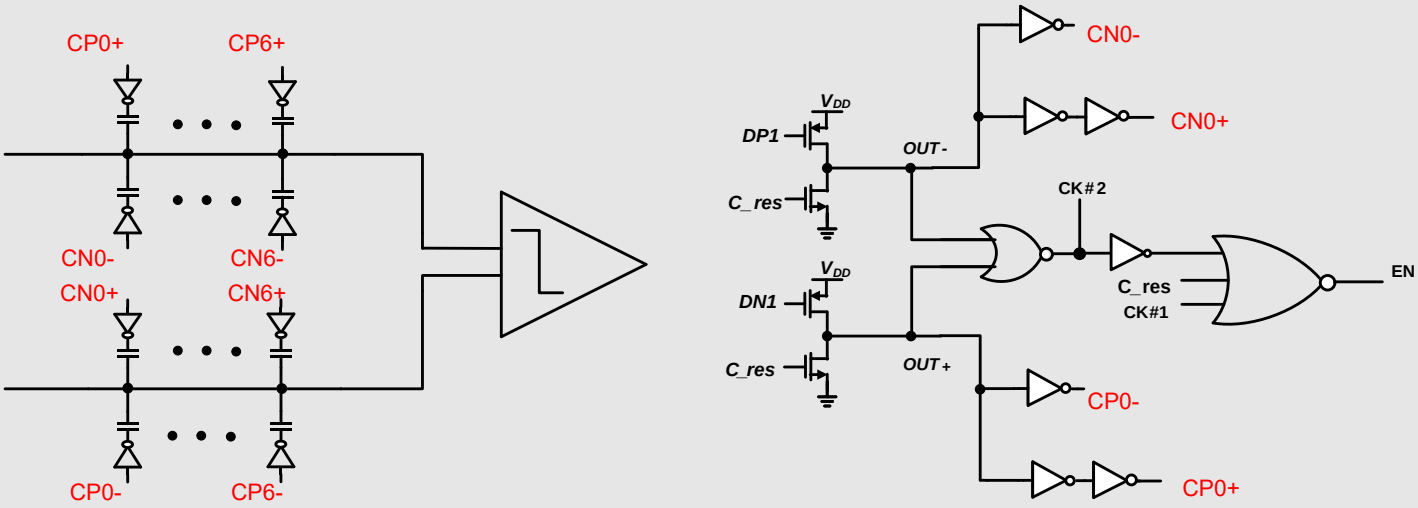

Figure 4.25 The connection between DAC and SAR logic

4.5 Simulation Results

4.5.1 T/H circuit simulation

As discussed in Section 4.1.3, dummy switches alleviate the effect of charge injection during sampling phase. Figure 4.26 shows the simulation of T/H with and without the dummy switch. The blue signal on the top is the sampling clock operating at 400MS/s; The green curve represents the input signal while the red one is the sampled signal. In Figure 4.26 (a), we can note that the voltage of sampled signal

is shifted caused by charge injection at the end of sampling. In contrast, the effect of charge injection is attenuated in the scenario where the dummy switch is used, as shown in Figure 4.26(b).

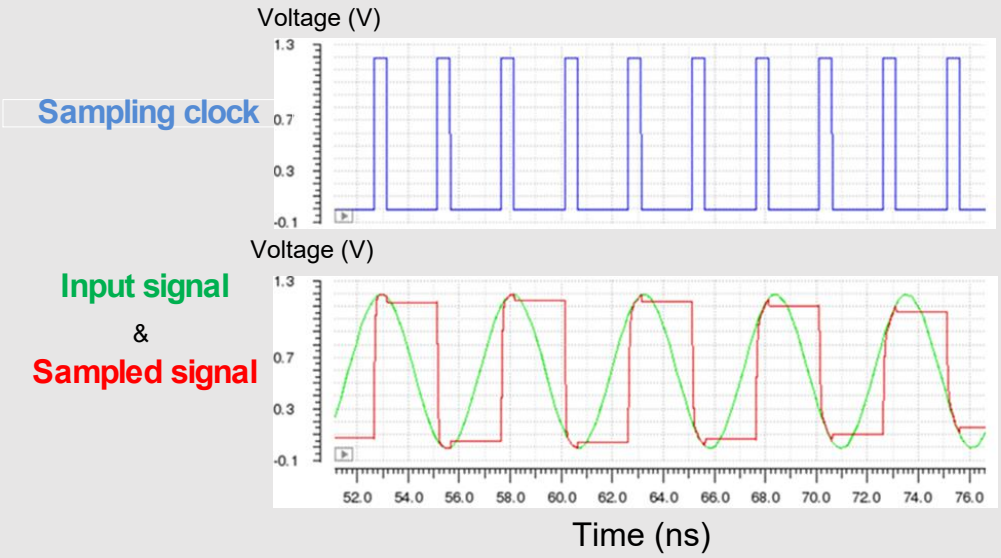

Figure 4.26 (a) CMOS T/H w/o the dummy switch

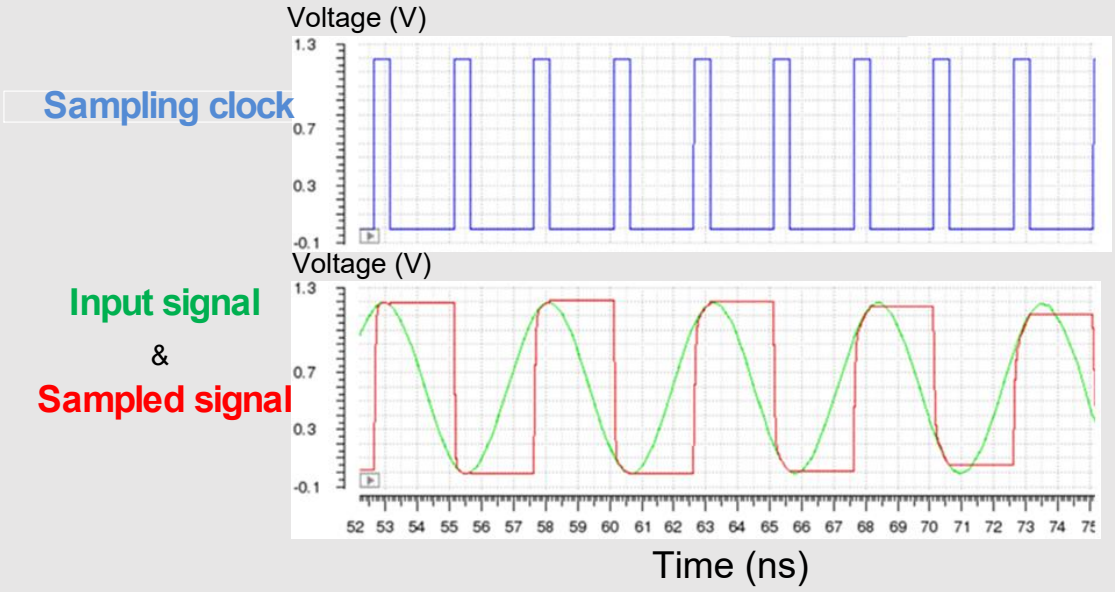

Figure 4.26 (b) CMOS T/H w/ the dummy switch

4.5.2 Concurrent comparator simulation

Figure 4.27 shows the enabling clocks of eight comparators during one conversion. Comparator are activated when the enabling clock rises and turned off when it falls. The falling edge of the previous

comparator clock crosses the rising edge of the subsequent one, which proves that the comparator is triggered without waiting for the previous comparator to be reset totally, thus the quantization speed is improved.

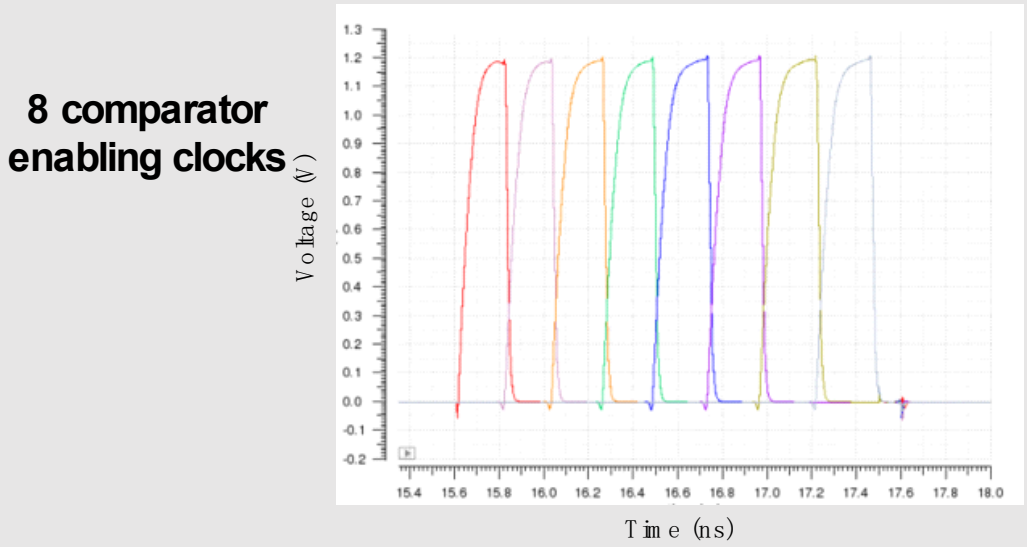

Figure 4.27 Enabling clocks of eight comparators

4.5.3 SNDR simulation

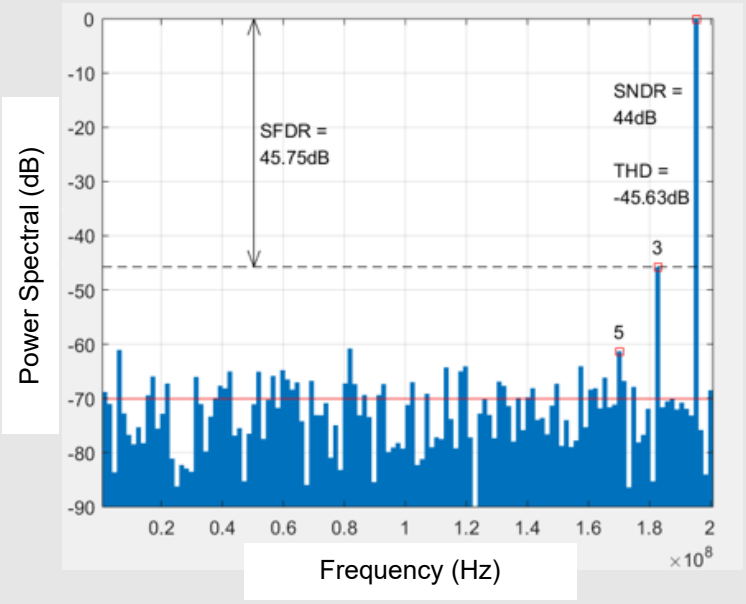

Figure 4.28 Frequency spectrum of proposed SAR ADC output (27 ℃, TT)

SNDR is simulated when the 8-bit SAR ADC operates at 400MS/s and the input frequency is 193.75Mhz. As shown in Figure 4.28, the ADC achieves an SNDR of 44dB at the process corner of 27 C°, TT (the environment temperature is 27C° and transistors work at a typical speed). By multiplying the supply voltage by the average current flowing through it, the power consumption is calculated as 530 μW. Compared to the 6-bit 300MS/s SAR ADC in [1], the proposed SAR ADC achieves a higher sampling frequency. One of the contributions to the improved conversion speed is the use of multiple concurrent comparators, which eliminates each comparator's reset time. Additionally, the removal of the DEMUX from the SAR logic enables the DAC to be reconfigured with simplified digital logics, enhancing the speed further.

At the process corner of 85C°, SS (When the temperature is at 85C° and transistors operate at slow speed), the ADC achieve an SNDR of 38.58dB, as shown in Figure 4.29.

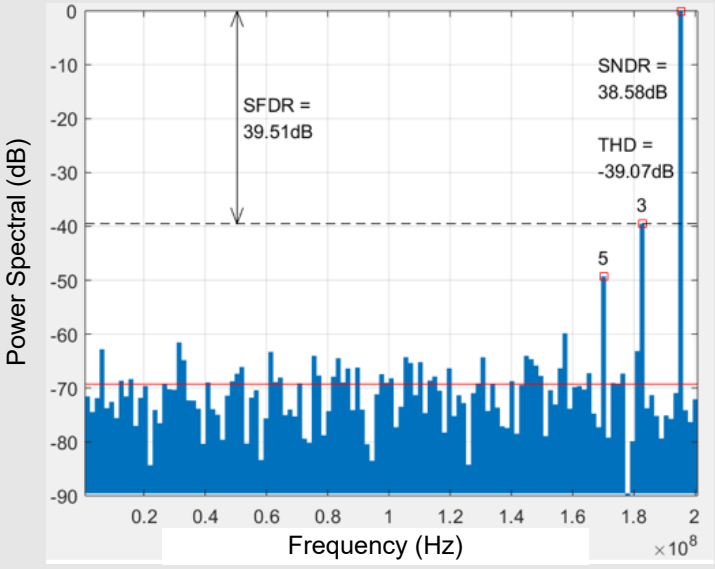

Figure 4.29 Frequency spectrum of proposed SAR ADC output (85 C°, SS)

From the above two spectra, we notice that the power of the third harmonic is high, limiting the SFDR and SNDR at different process corners. The harmonic distortion mainly comes from the T/H circuit. If it is replaced with an ideal switch, the power of harmonics is reduced and the SNDR is improved to 47.61 dB (27 C°, TT) as shown in Figure 4.30. In order to improve the SNDR, bootstrapped T/H circuits can be used in the future work, which can provide better linearity than CMOS T/H.

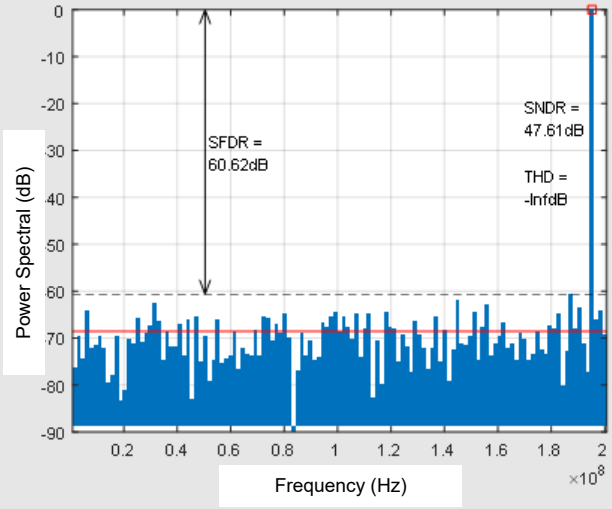

Figure 4.30 Frequency spectrum of proposed SAR ADC with ideal T/H(27 C°, TT)

Chapter 5

Conclusion and Future Work

5.1 Conclusion

SAR ADCs have gained wide usages in many ADC applications due to its power efficiency and high performance. This thesis presents an architecture of SAR ADC with speed enhancement. CMOS T/H circuits and dummy switches are utilized to provide high linearity and compensate the charge injection. Using one comparator for each decision results in higher conversion speed because every comparison can be triggered before the previous one is reset completely. In addition, the DEMX is removed from the digital logic because each comparator drives only one set of DAC capacitors, thus the speed of DAC reconfiguration is increased. The 8-bit SAR ADC is designed in 65nm CMOS technology and achieves an SNDR of 44dB at 400MS/s for a Nyquist input while consuming 530μW. A higher conversion speed is accomplished compared to the previous work [1] due to the use of multiple concurrent comparators and the removal of the DEMUX. The SNDR is limited by harmonic distortions, which mainly come from the sampling circuit. So bootstrapped circuits can be used in the future work to improve the ADC resolution.

5.2 Future work

It is difficult for SAR ADCs to reach higher resolution than 12 bits. One of the reasons is the comparator noise becomes much larger in LSB conversion steps. For example, assuming full-scale differential inputs are fed to an 8-bit SAR ADC where the reference voltage is 1.2V. V_{ip} is greater than V_{in} by only 9.375mV after conversion, as shown in Figure 5.1. For ADCs with higher resolution like 12

bits, the voltage difference fed to comparators is even smaller, resulting in higher possibility of comparator giving wrong decisions due to the noise effect.

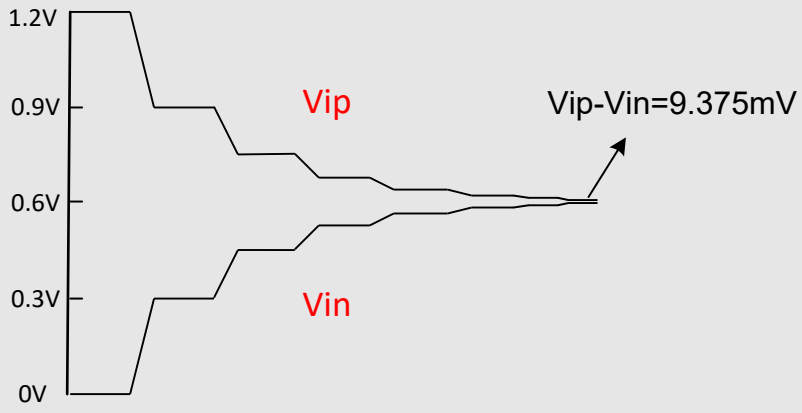

Figure 5.1 Conversion of V_{ip} and V_{in} in SAR ADC *Figure 0-2*

Then the question is: what if (V_{ip}-V_{in}) is amplified during the convergence? Figure 5.2 indicates this case and the voltage difference after conversion is 46.875mV (gained by 5 times).

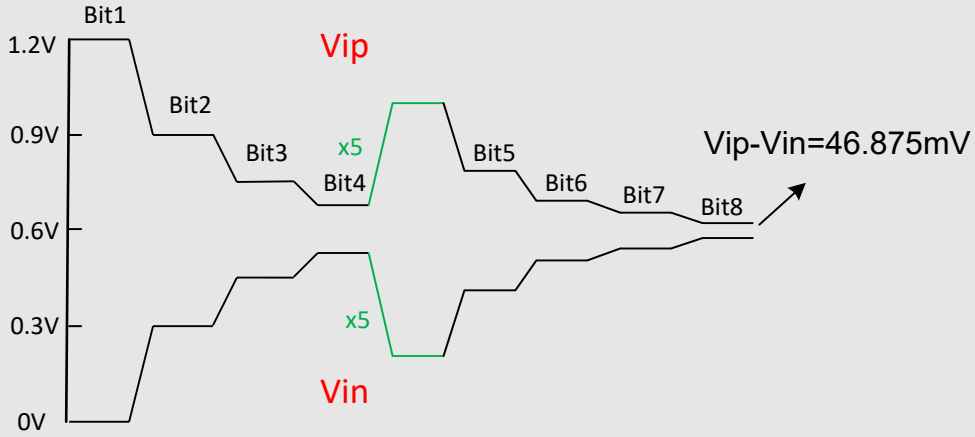

Figure 5.2 Conversion of V_{ip} and V_{in} in Pipelined SAR ADC

Due to the amplification, the noise effect is comparatively smaller and higher resolution can be achieved. This structure is called “Pipelined SAR” ADC, and its block diagram is depicted in Figure 5.3. The pipelined SAR ADC is composed of two SAR ADCs and a residual amplifier in between. Even

though extra time is needed for amplification, the total speed of ADC is not degraded since two stages are pipelined and work in parallel. A high-performance Pipelined SAR ADC design is in progress and the architecture of each stage is based on the SAR ADC in this thesis. In addition, the time-interleaving technique is used to achieve higher sampling rate at the range of Giga Samples/second.

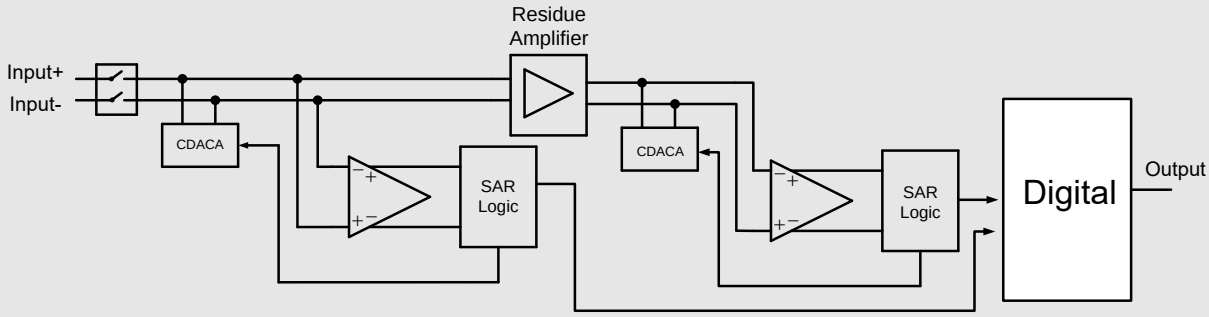

Figure 5.3 pipelined SAR ADC block diagram

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