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On-Chip Nonreciprocal Components for Full-Duplex Communications and Gaussian Regulated Gate Driver for Electromagnetic Interference Reduction

Chang Yang
Southern Methodist University, changyang@smu.edu

ON-CHIP NONRECIPROCAL COMPONENTS FOR FULL-DUPLEX COMMUNICATIONS AND GAUSSIAN REGULATED GATE DRIVER FOR ELECTROMAGNETIC INTERFERENCE REDUCTION

Approved by:

Prof. Ping Gui
Professor of Electrical Engineering
Dissertation Committee Chairperson

Prof. Ron Rohrer
Professor of Electrical and Computer Engineering

Prof. Theodore Manikas
Clinical Professor of Computer Science

Prof. Joseph Camp
Associate Professor of Electrical and Computer Engineering

Prof. Choon Lee
Associate Professor of Electrical and Computer Engineering

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Chang Yang

M.S., Electronics Science and Technology, University of Electronic Science and Technology of China, Chengdu
B.S., Electronics Science and Technology, Liaoning University Shenyang

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Yang, Chang M.S., Electronics Science and Technology, University of Electronic Science and Technology of China, 2012 Chengdu
B.S., Electronics Science and Technology, Liaoning University, 2008 Shenyang

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This dissertation is comprised of two unrelated design endeavors. The first one is about two CMOS nonreciprocal components: 1) an isolator and 2) a circulator. To make the components compact enough for the next generation communication systems with wide bandwidth, both components operate at 100 GHz band for full-duplex transceivers for ultra-high-data-rate millimeter-wave wireless communication. The proposed nonreciprocal structures are based on a time-domain modulation by signals at around 1/6 of the RF frequencies and spatial duplexing over the RF signal paths, demonstrating over 45 dB isolation in a bandwidth of 1.5 GHz over the tuning range of 85-110 GHz. In the presented isolator, two capacitive mixers together with a biasing network form a resonant type of wideband matching network for lower loss. An enhanced delta topology is proposed for the circulator design which reduces the design complexity and chip area overhead. Implemented in a 65 nm CMOS with a chip area of 0.13 mm^2 and 0.21 mm^2, respectively, both the isolator and the circulator achieve over 45 dB isolation and better than 10 dB return losses throughout the entire bandwidth. A maximum 4.5 dB and 5.6 dB insertion losses (ILs) are achieved by the isolator and circulator, respectively.

The second design endeavor aims at Electromagnetic Interferences (EMI) suppression on DC-DC power converter, especially for the Gallium Nitride (GaN)-based buck converters which operate at high switching frequencies but with high level of EMI noises. A Gaussian

switching scheme is realized on chip for the first time for GaN power switches to effectively reduce the EMI level in the high-frequency domain. Meanwhile, spread-spectrum frequency dithering (SSFD) technique is adopted to compress the spurious switching noise in the low-frequency domain. In order to handle high-speed Gaussian switching, a feed-forward segmented driving scheme is proposed to generate precise Gaussian trajectories. The Gaussian slopes are reconfigurable to enable optimization of the power efficiencies for different EMI standards. Implemented in a 180 nm High voltage CMOS process, the presented GaN-based buck converter reduces EMI noise by 36.9 dB and 49.1 dB at 10 MHz and 100 MHz respectively. From 250 MHz to 400 MHz and from 400 MHz to 500 MHz, the measured peak EMI noise is reduced by 22 dB and 16 dB, respectively. While the EMI is greatly reduced, the maximum power efficiency is 85.2%, comparable to that of other state-of-the-art GaN gate driving schemes.

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Chapter 1

Introduction

1.1 Nonreciprocal Components for Full-duplex Transceivers

As data traffic in wireless systems continues to grow exponentially, enhancing spectral efficiency and channel capacity is becoming increasingly critical in both commercial and defense applications. Full duplex wireless systems operating at millimeter wave (mm-wave) and sub-TeraHertz (sub-THz) regimes are key technologies for next-generation wireless communication systems. As shown in Fig. 1.1, full-duplex communication allows the transmitter and receiver to operate at the same frequency simultaneously, thereby doubling the spectral efficiency in the physical-layer compared to the half-duplex schemes such as time-division duplex (TDD) and frequency-division duplex (FDD) [1–4]. Moreover, the full-duplex scheme offers many potential benefits in the access-layer. It can alleviate scheduling constrains from half-duplex such as self-collision, hidden node problem and the resulted energy dissipation [5, 6].

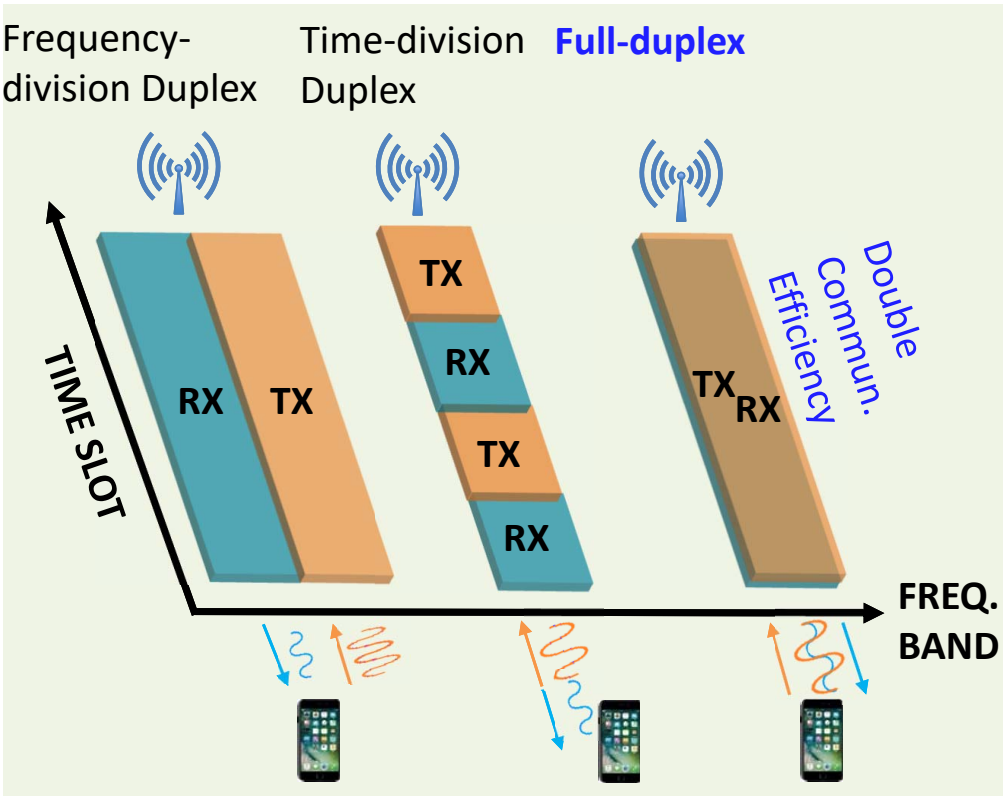


Figure 1.1: Spectral efficiency comparison between time-division duplex (TDD), frequency-division duplex (FDD) and full-duplex.

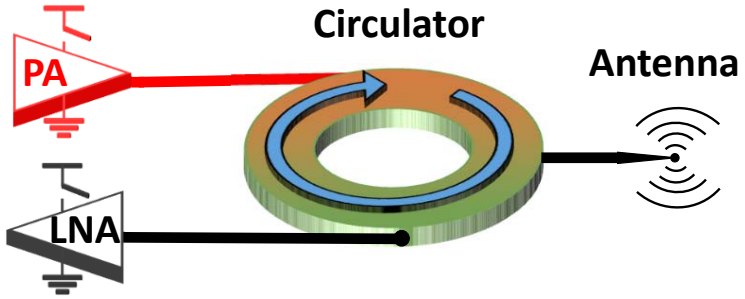


Figure 1.2: Circulator-based wireless transceivers (TRXs) for full-duplex communication.

Full-duplex wireless full-duplex transceivers (TRXs) are also desirable at mm-wave radar/ imaging applications. By eliminating the offsets from the separate antennas, the cross-range accuracy can be increased in a full-duplex continuous-wave radar or sub-THz imaging TRX with a single shared antenna [5, 7].

Full-duplex TRX can be realized using nonreciprocal components such as circulators or isolators. As shown in Fig. 1.2, circulators can directly provide the antenna interfaces to separate the transmitting and receiving paths with high isolation, while ensuring low insertion loss. On the other hand, the circulator function can be realized using isolators in combination with common hybrid couplers as well [8, 9]. In the full-duplex applications, high isolation and low insertion loss (IL) at mm-wave/sub-THz frequencies are the key design parameters. In addition, good large-signal performance is necessary for these two components to feed the RF signal to the antenna without distortion.

1.2 Electromagnetic Interferences (EMI) from GaN-based DC-DC converter.

Emerging technologies for automotive, motor drivers and communications have pushed the power density of power converters to an unprecedented level. Gallium-Nitride (GaN) devices are attractive alternatives to displace silicon power devices because of their higher converting power level and switching frequency (f_{SW}) thanks to their smaller total gate charge and much lower source-drain on-resistance [10, 11]. Due to their small gate charge, they enable much shorter switching transition and higher switching frequency [12, 13]. For switching power converters, lower ON-resistance allows for higher power levels. However, as f_{SW} and the power level increase, more electromagnetic interferences (EMI) are generated from the switching node voltage (shown as V_{SW} in Fig. 4.2). These EMI noise would propagate along the power line and jeopardize other sensitive on-board devices as shown in Fig. 1.3. Analysis on the switching behavior and its resulting spectrum reveals that there exist multiple EMI sources located at different frequency bands in a power converter [14]. First of all, the intrinsic harmonic components in the spectrum of the ideal trapezoidal switching signal V_{SW} is one major EMI source. Additionally, as the frequency/slew rate of V_{SW} increases, the I/V overshooting and ringing caused by the parasitic inductance and capacitance (LC) and body diodes in the power switches become more severe. This would

cause excessive distortions on V_{SW} during each cycle and introduce EMI in the high-frequency domain. These EMI noises are injected into the input power bus, and may interfere with and jeopardize the sensitive on-board devices operating at radio frequencies, Bluetooth, Wi-Fi or cellular bands.

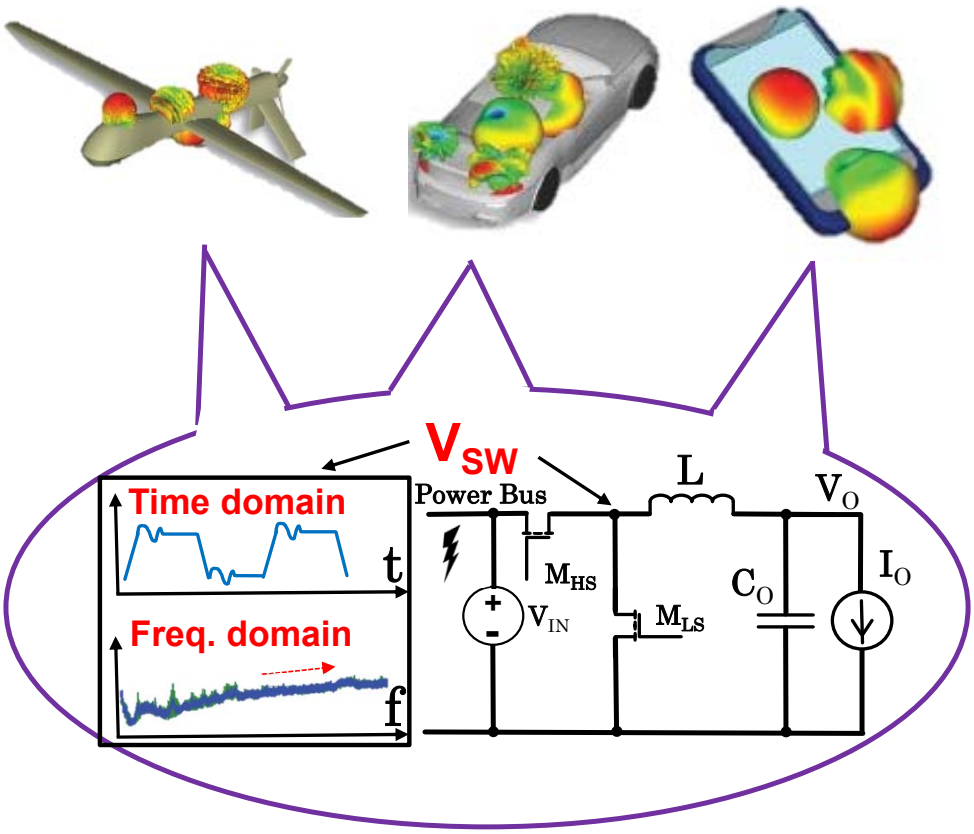


Figure 1.3: Conducted EMI noise generated from power converters.

1.3 Dissertation Organization

The dissertation is organized as follows. Chapter 1, research scopes of proposed work are introduced. Chapter 2, the background and existing work of nonreciprocal components is illustrated. Chapter 3, the operation principle, design details and experimental results of the proposed nonreciprocal components are analyzed and presented. Chapter 4, background

and existing work of Gaussian switching regulation for EMI reduction are analyzed. In Chapter 5, the characterizations of the GaN-based on-chip Gaussian switching regulation are firstly described, followed by the design details and experimental results of the proposed Gaussian gate drivers. Conclusion and future work of the proposed designs are summarized in Chapter 6.

Chapter 2

Motivation for Magnetic-free Nonreciprocal Components and Research Contribution

2.1 Background and Existing Work of Nonreciprocal Components for Full-duplex Communication

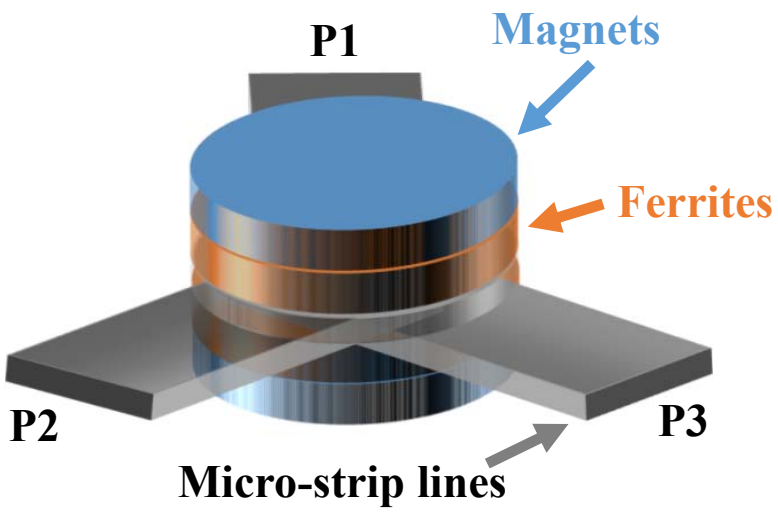


Figure 2.1: Structure of the conventional magneto-optical-media-based circulator.

Conventionally, nonreciprocal components are fabricated with magneto-optical media such as ferrite under magnetic biasing typically provided by magnetic material as shown in Fig. 2.1. These structures are bulky, lossy and incompatible with CMOS IC fabrication processes. Active devices are inherently non-reciprocal, but they are severely limited in their linearity, isolation and noise performance.

Recently, the theory of spatio-temporal modulation has been proposed and formulated to

design magnetic-less non-reciprocal components [8, 9, 15–24]. By leveraging parametrically modulated mixing stages distributed along a transmission path, the frequency mixing and spatial duplexing property of the time-varying structure can break the Lorentz reciprocity and only allow signals to transmit in one direction through a medium as shown in Fig. 2.3. This approach requires only transistors and passive components such as inductors, capacitors which are feasible to realize on chip while providing good isolation to replace the conventional circulators or isolators.

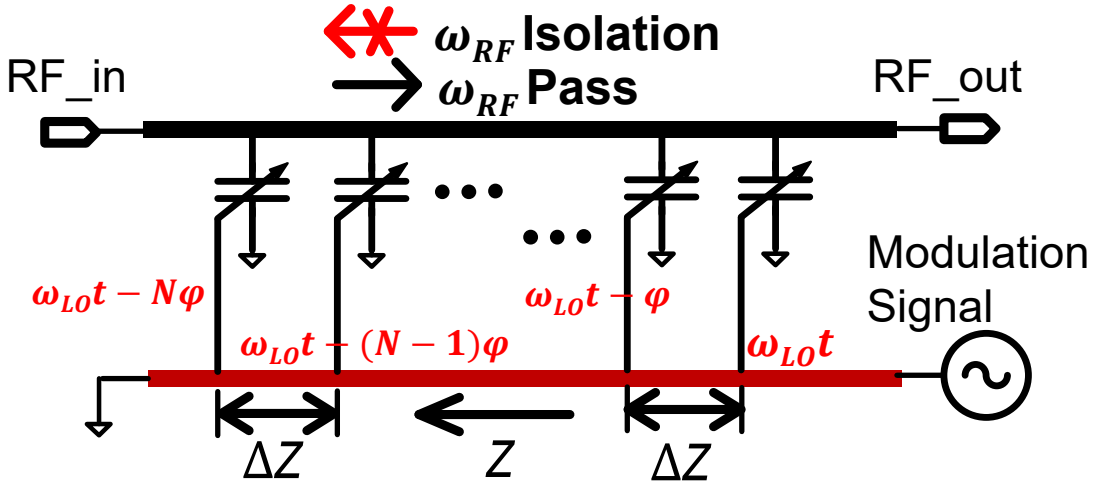


Figure 2.2: Structure of published spatio-temporal-modulation-based isolator.

This concept has been exploited in the low-RF frequency regime. References [9, 18, 25] present the structures of isolators using nonreciprocal transmission lines (NTLs) based on travelling-wave structures. As shown in Fig. 2.2, the shunt mixing stages are distributed along the RF signal path at angular frequency ω_s. The modulation stages are driven by a high-side modulation signal of ω_m which is greater than ω_s. Both the modulation signal path and RF signal paths are bulky travelling wave structures and connected in double-balanced manner which will introduce excessive losses making it not amenable for mm-wave/sub-THz operation.

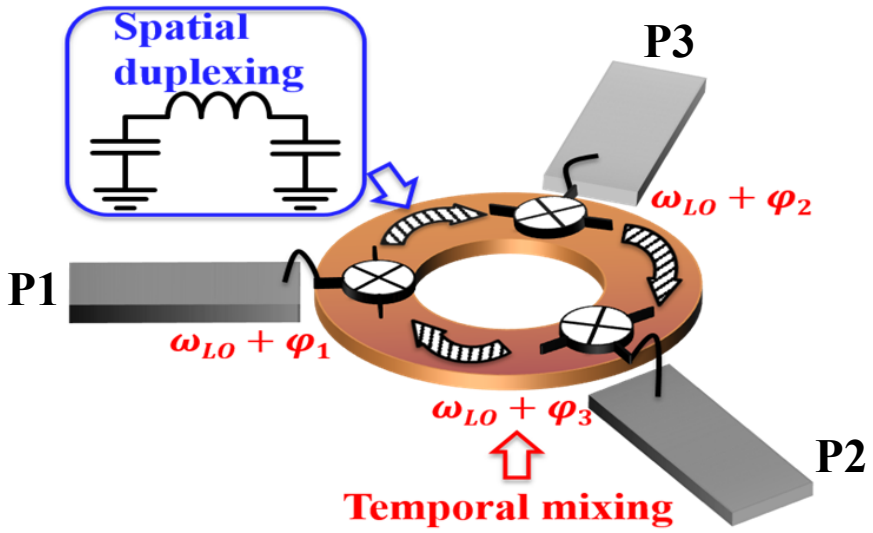


Figure 2.3: Idea of spatio-temporal-modulation-based circulator.

As for the circulators, two categories of magnetic-less circulators have been reported in prior arts as shown in Fig. 2.4. One type is based on resonant-type ring or Y-shape modulation stages [16, 19, 20], which have relatively simple architectures and are feasible to implement in silicon for low-GHz operation. These works so far have been demonstrated operating at around 2 GHz at the PCB level. The other type is based on non-resonant modulation stages such as staggered commutated network or Gilbert mixers, which can operate at 25 GHz on chip [17, 21–23].

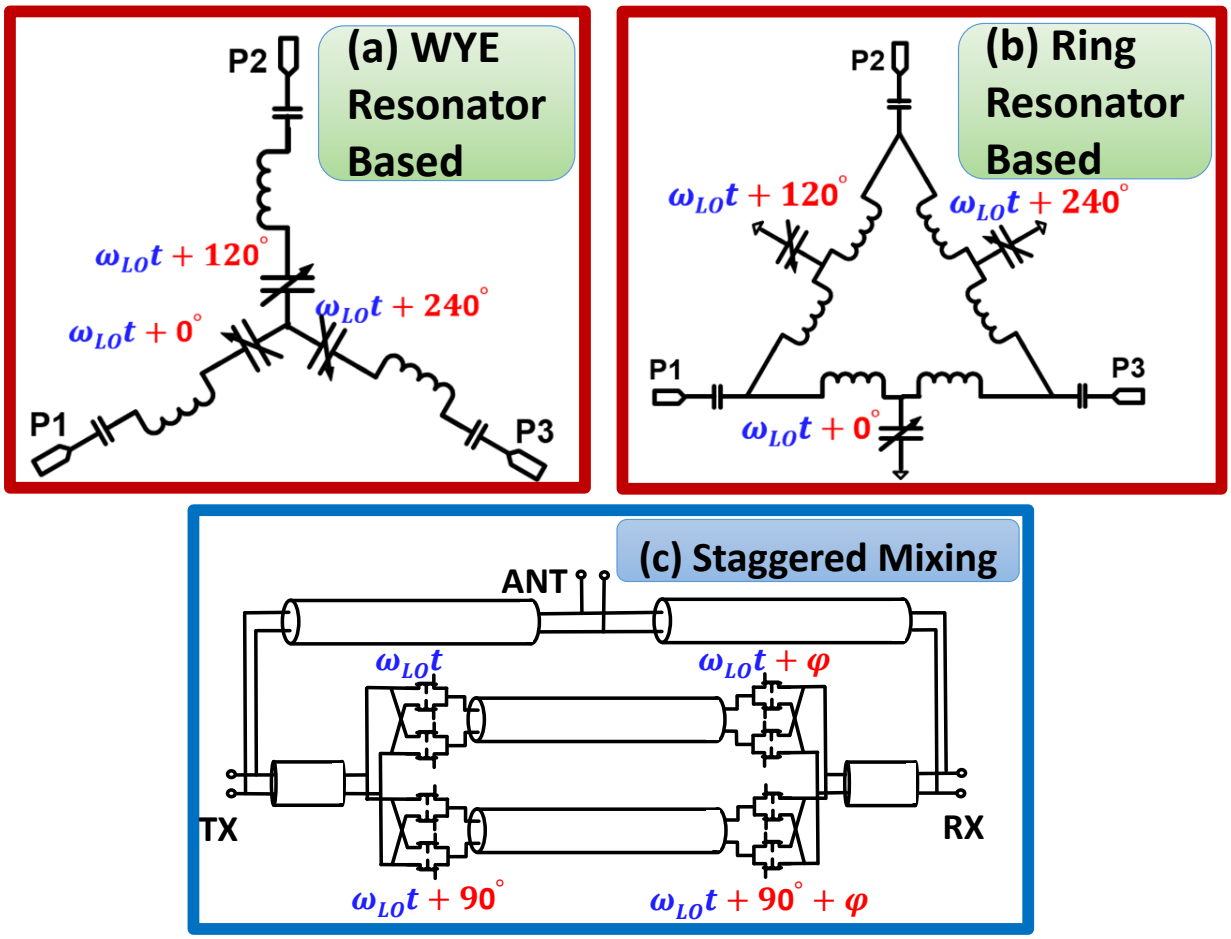


Figure 2.4: Structures of published spatio-temporal-modulation-based circulators: (a)WYE resonator based circulator, (b) ring resonator based circulator and (c) Mixer based circulator

At higher frequencies of the mm-wave and sub-THz bands, the modulation elements experience lower conversion gain due to the degradated g_m of the transistors and undesired attenuation loss, resulting in excessive insertion loss and noise which will be more obvious towards higher frequencies. Moreover, at higher frequencies mismatch would become more severe due to PVT variations resulting in failure to meet the required phase-shifting for the spatio-temporal modulation.

2.2 Original Contribution

This dissertation presents new techniques that allow magnetic-less circulators and isolators to operate on-chip at mm-wave frequencies while providing higher isolations and low

insertion loss. First, the spatial duplexing is provided by on-chip TLs and inductors where the fundamental signals and their sidebands propagate through. The on-chip resonant tanks are selected as the mixers which has optimized conversion gain. Second, to generate the frequency mixing signals, in the isolator, the local oscillator (LO) delay line is fabricated by TL network in each of the mixing stages. Third, to minimize the insertion losses, a novel serially resonant structure for frequency mixing is presented for the isolator. As for the circulator, the TL structure for spatial duplexing between each of the two mixers is utilized as part of the matching network to reduce the insertion loss and design complexity.

The full-duplex TRX can be used in wireless IO in data center for ultra-high-data-rate communication in short distance. The license-free 100 GHz band is chosen as the operation frequency to avoid occupying the E-band (70-90 GHz) which is used by wireless backhaul and automotive radars. A low-side mixing is chosen as the temporal modulation scheme ($\omega_m < \omega_s$). Readily integrable in CMOS process when operating at 100 GHz band, these devices enable full-duplex TRXs to be entirely embedded on chip.

Chapter 3

Proposed CMOS Magnetic-free Nonreciprocal Components Using Spatio-temporal Modulation

3.1 Theory and Proposed Circuit Topologies

3.1.1 Proposed Isolator

3.1.1.1 Circuit Topology

We present a serial resonant topology for the isolator and demonstrated it at 100GHz band [8]. As shown in Fig. 3.1, a varactor (M1 $\neq$ M2) in parallel with an inductor (L1 = L2) works as a capacitive mixing stage. Two of such mixing stages with different resonance frequencies are connected back-to-back to form a serial resonant network for the RF signal of frequency ω_s. Dispersive spatial duplexing circuit consists of the two inductors which are shared by the two mixing stages and the TL line in between them. The two varactors M1 and M2 are modulated by a low-side modulation signal (LO) at an angular frequency of ω_m along the same direction as the RF signal, from the RF_in to the RF_out port.

To block the LO leakage, high-pass filters (HPFs) are employed at the input and output of the RF path. To prevent the RF signal from leaking through the LO modulation path, band-stop LC tanks resonating around ω_s are placed at the input and the output of LO signal path.

Different from the existing spatio-temporal modulated isolator in [9,18,25], there are three major highlights in the proposed isolator. First, it achieves self-isolated RF signal path by utilizing only two modulation stages to prevent RF feedthrough at mm-wave frequencies. Second, the single-ended operation mode reduces the size of the schematic by half, therefore reducing the power consumption and chip area. Meanwhile, the serial resonance provides low TX-ANT IL at resonance, minimizing insertion loss. The Q-factors of the LC tanks

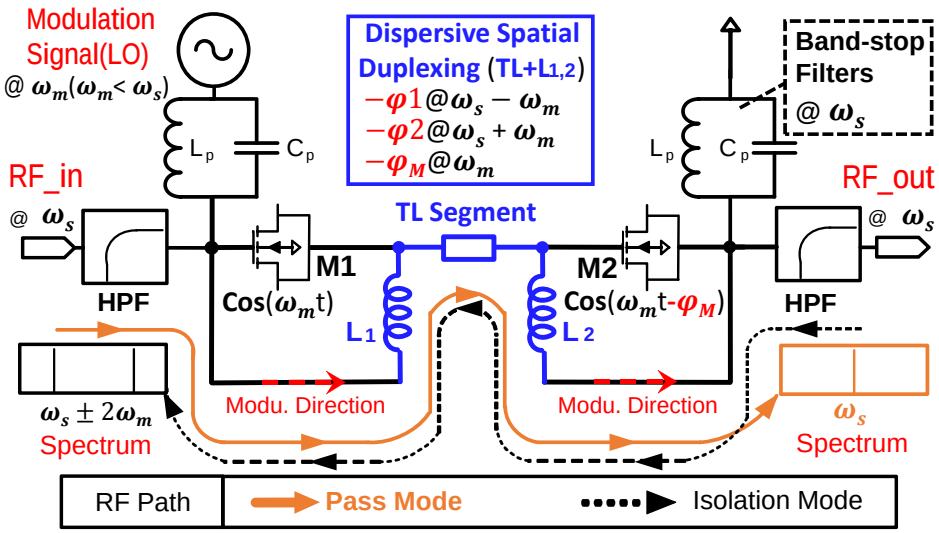


Figure 3.1: Proposed structure of the isolator with two serial capacitive mixing stages.

listed in Table 3.1 can be utilized to estimate the real resistance across the serial resonators which is about 2 Ω to 8 Ω.

3.1.1.2 Operation Principle

The frequency modulation (mixing) theory is employed to illustrate the isolator operation principle [24]. Compared to the conventional Telegrapher's equation theory analysis [8, 26], the mixing theory approach can determine the exact phase delays of the modulation signals. Moreover, the method is suitable for both nondispersive and dispersive nonreciprocal structures which renders the approach more precise and universal.

Fig. 3.2 depicts the signal propagation through the proposed isolator in two operation modes. The two parallel LC tanks are modelled as two parametric mixers in which the RF signal at an angular frequency of ω_s multiplies (mixes) with the sinusoidal LO signal at ω_m. Through the proposed isolator, the RF signal of ω_s is mixed with the low-side modulation signal ω_m twice by the two parametric mixers.

In the pass mode when the RF signal ω_s is injected from the *RF_in* to the *RF_out* port, the parametric mixer #1 produces two side bands at $\omega_s + \omega_m$ and $\omega_s - \omega_m$. The RF path between the two mixers then introduces phase delay of $-\varphi_1$, $-\varphi_2$ and $-\varphi_M$ on the two side bands of $\omega_s - \omega_m$ and $\omega_s + \omega_m$ as well as on the modulation signal of ω_m, respectively.

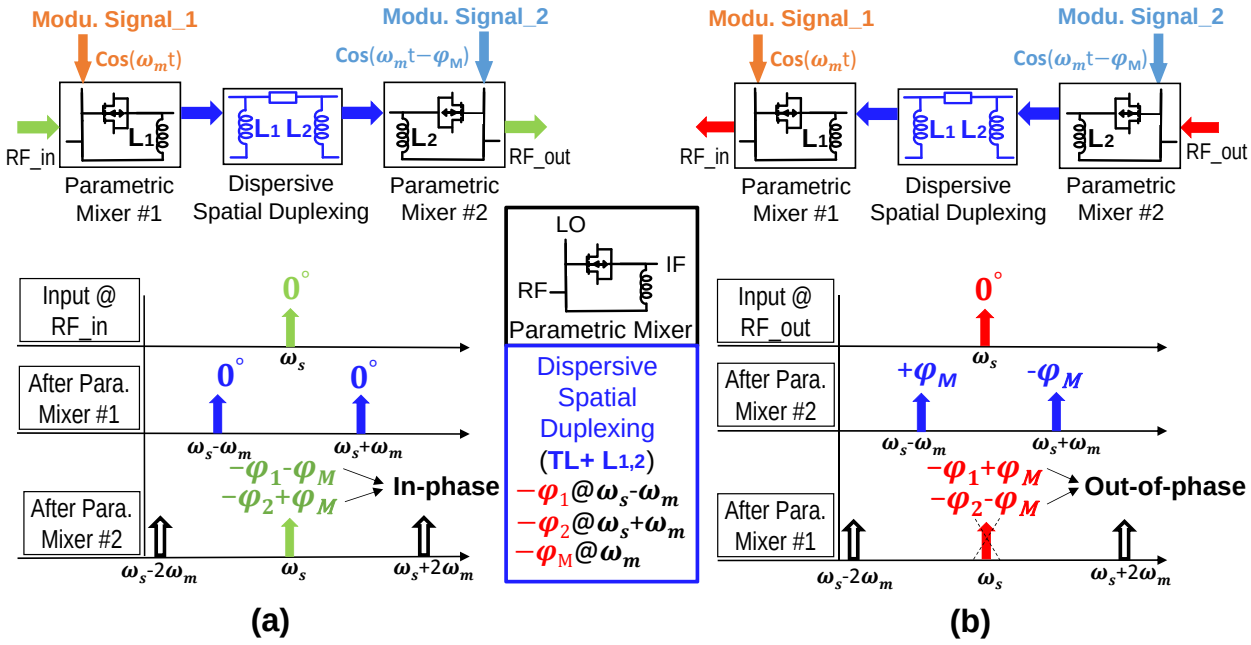


Figure 3.2: Operation principle of the proposed isolator in Frequency Mixing Theory: (a) pass mode, (b) isolation mode.

The phase delay through the RF path essentially realizes the spatial duplexing. The phase delay of the RF path is largely determined by the path length and the capacitance of the varactors loaded on the RF path [16, 26]. Afterward, mixer #2 produces four side bands, two at $\omega_s \pm \omega_m$ and the other two exactly at ω_s. The isolator is designed in such a way that the two side bands produced at ω_s have the same phase delay, thus adding up constructively to produce the RF signal at ω_s in the pass mode.

Contrarily, in the isolation mode when the RF signal is input at the RF_out port, parametric mixer #2 first produces two side bands at $\omega_s - \omega_m$ and $\omega_s + \omega_m$. These side bands experience phase delay of $-\varphi_1$ and $-\varphi_2$, respectively through the RF path between the two mixers. Then parametric mixer #1 then produces four components, two at $\omega_s \pm 2\omega_m$, and the other two at ω_s with different phases. The isolator can be designed such that the phases of the two components at ω_s will be opposite of each other, canceling out each other resulting in zero signal at ω_s in the isolation mode.

The conditions to produce both in-phase summing and out-of-phase summing simultaneously for the pass mode and isolation mode can be expressed as follows:

$$\begin{cases} cos\left(\omega_s t + \dfrac{-\varphi_1 - \varphi_2}{2}\right) cos\left(\dfrac{-\varphi_1 + \varphi_2 - 2\varphi_M}{2}\right) = 1 & \text{(3.1a)} \\ cos\left(\omega_s t + \dfrac{-\varphi_1 - \varphi_2}{2}\right) cos\left(\dfrac{-\varphi_1 + \varphi_2 + 2\varphi_M}{2}\right) = 0. & \text{(3.1b)} \end{cases}$$

From (3.1b), it can be observed that in the isolation mode, the output becomes zero, meaning that the RF signal is isolated. On the other hand, in the pass mode according to (3.1a), the components at ω_s add up constructively into a single signal without phase mismatch and the isolator exhibits ideal nonreciprocal transmission property. The exact values of φ_1, φ_2 and φ_M can be obtained by simplifying (3.1a) and (3.1b) to (3.2) as

$$\begin{cases} \left| cos\left(\dfrac{-\varphi_1 + \varphi_2 - 2\varphi_M}{2}\right) \right| = 1 & \text{(3.2a)} \\ cos\left(\dfrac{-\varphi_1 + \varphi_2 + 2\varphi_M}{2}\right) = 0. & \text{(3.2b)} \end{cases}$$

Under the constrains of low-side modulation scheme where $\omega_m < \omega_s$, (3.2a) and (3.2b) can be solved for the phase delay requirements for φ_M, φ_1 and φ_2 to achieve pass in one direction and isolation in the other. One feasible solution with the minimum length of the RF signal path is $\varphi_M = 45°$, $\varphi_1 = 135°$ and $\varphi_2 = 225°$. Under these phase delay conditions the proposed isolator achieves an ideal nonreciprocal propagation.

3.1.2 Proposed Circulator

The frequency modulation theory in the proposed isolator can be applied to circulator as well. Three capacitive mixing stages based on varactors corresponding to three RF signal pathes in the circulator are utilized to provide the temporal modulation. The TL segments with certain lengthes are used to connect the three mixing stages meanwhile providing a major part of the spatial duplexing. Resonate-type topology similar to the proposed isolator [16,19] is adopted to the mixing stages for its robust structure to tolerant phase mismatches caused by the PVT variations and small chip footprint. However, higher conversion gain of the circulator are needed to combat the huge attenuation loss at the hundreds of GHz band.

In the existing resonant-type topology [16, 19], there is a frequency-dependent conversion loss at around 0.8 dB owing to the conventional modulation-signal phase delays at 0°, 120° and 240° [16, 19].

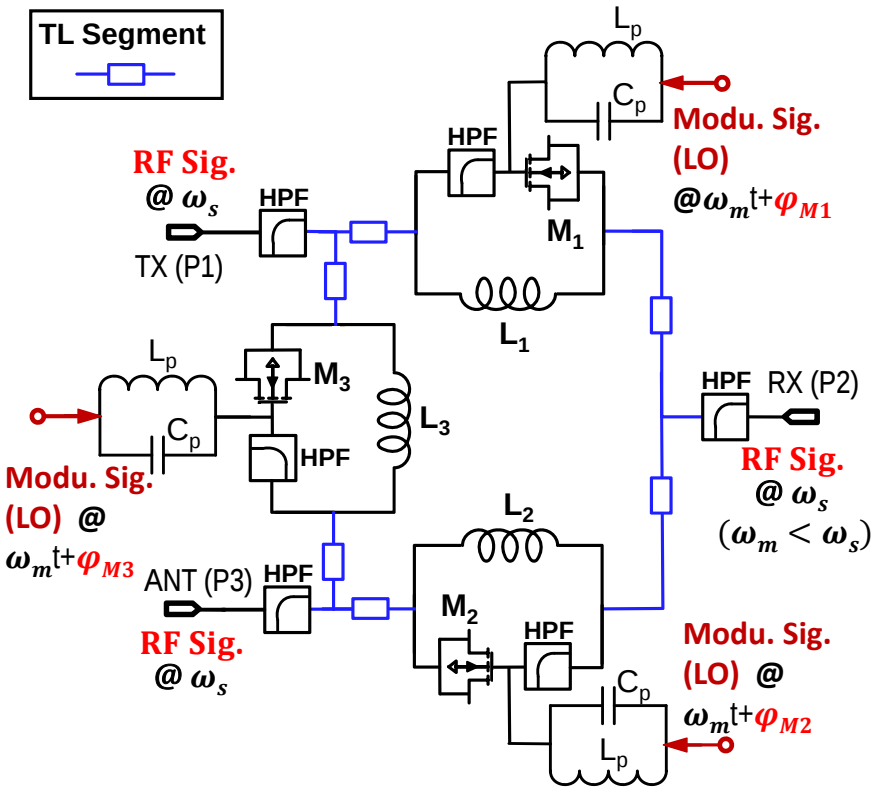


Figure 3.3: Proposed structure of the circulator with parallel LC tanks resonating around RF frequency.

3.1.2.1 Circuit Topology

The schematic of the proposed resonant-type circulator is depicted in Fig. 3.3. The circuit comprises three identical parallel LC tanks connected side by side in a delta manner. These tanks serve as mixing stages operating around the same resonating frequency of f_s, which is given by

$$f_s = \frac{1}{2\pi\sqrt{LC_s}} \tag{3.3}$$

where L and C_s are the total inductance and capacitance of the parallel LC tank, respectively. During the time-varying modulation in this resonant-type circulator, C_s variation is achieved via varactors being continuously modulated by a sinusoid modulation signal around the DC operating point. The tanks′ resonance frequencies, therefore, vary from time to time. The three modulation signals have the same angular frequency ω_m and amplitude, but with phase differences between different tanks as required in the temporal modulation approach. The spatial duplexing is mostly provided by three segments of TLs between each of the two mixing stages, which also form the major part of the matching network towards three RF ports P1, P2 and P3, respectively.

In the proposed isolator, two parametric mixers together with the TL in between them resonate serially at RF frequency exhibiting low impedance between the two RF ports to eliminate additional matching networks. On the other hand, the proposed circulator has the parallel LC-tanks which show high impedance (380 Ω at 100 GHz) at the RF frequency. According to Fig. 3.3, right between the parallel LC-tanks and the RF ports there exist TLs which provide an important part of the spatial duplexing. Consequently, these TLs are absorbed into the matching networks to match the impedance at each of the RF port to 50 Ω.

This dissertation demonstrates for the first time resonant-type nonreciprocal components on-chip to achieve more than 45 dB isolation at mm-wave regime. The varactors are driven at cathode nodes. A high-pass filter (HPF) made of inter-digital metal capacitors is connected to the varactor cathode to improve the driving strength and prevent the modulation signal from leaking through the modulation stages. Similar to the proposed isolator, the parallel LC tanks resonating around ω_s and HPFs are used to eliminate the RF leakage and LO leakage, respectively.

3.1.2.2 Operation Principle Using Frequency Mixing Theory

Conventionally, the resonant-type spatio-temporal modulated circulators are analyzed by solving linear small-signal response equations in coupled networks [19]. With this approach, second-order partial differential equations have to be solved with very large scale matrix involving many variables. Moreover, the method fails to analyze the situations when the

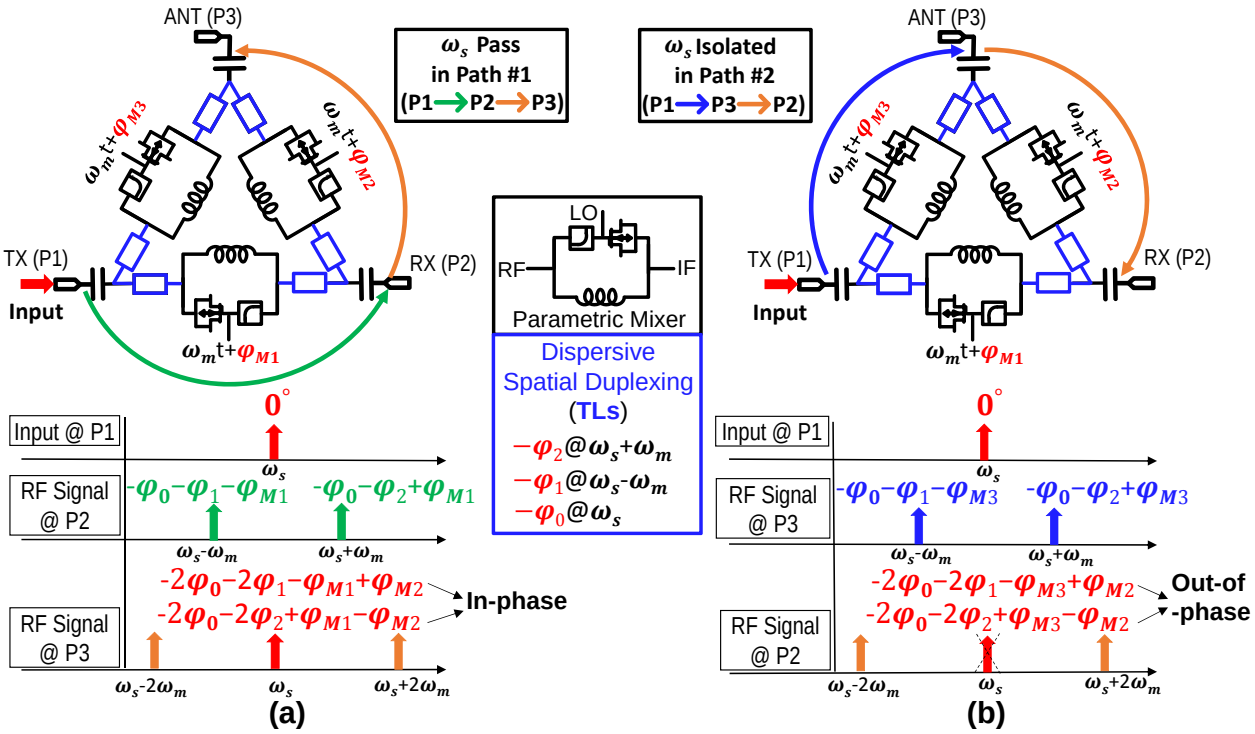


Figure 3.4: Operation Principle of the proposed circulator in Frequency Mixing Theory: (a) pass mode, (b) isolation mode.

phases of the modulation signals are not at values of 0°, 120°, and 240°, respectively.

In this dissertation, the mixing-theory approach, which is similar to that used in the isolator analysis, is extended to analyze the three-port, resonant-type circulators with flexible phase modulation schemes. It is shown that, a low-loss spatio-temporal modulation is achieved by optimizing the modulation scheme. The theory is validated with circuit simulation results and measurement results in Section 3.2 and 3.3 in this dissertation.

Using the mixing theory, the operation principle of the proposed circulator can be illustrated as shown in Fig. 3.4. P1, P2 and P3 are the three RF ports of the circulator. The pass mode is defined as the case when the RF signal propagates from P1 to P3 through P2, and the isolation mode is when the RF signal transmits from P1 to P2 through P3. The three parallel LC tanks are modelled as parametric mixers the same way as in the isolator. To provide spatial duplexing, TLs are connected between the RF ports and mixing stages, and the phase delays for frequencies $\omega_s + \omega_m$, $\omega_s - \omega_m$ and ω_s are generated by the TL segments

and are denoted as $-\varphi_2$, $-\varphi_1$ and $-\varphi_0$, respectively. To explore the optimum modulation solution, each of the three LO signals has its own phase, denoted as φ_{M1}, φ_{M2} and φ_{M3} as shown in Fig. 3.4.

In the pass mode when an RF signal at $\omega_s t + 0°$ is input from P1, two sidebands at $\omega_s \pm \omega_m$ are generated by the mixing stage with two distinct phase delays, $-\varphi_0 - \varphi_1 - \varphi_{M1}$ and $-\varphi_0 - \varphi_2 + \varphi_{M1}$, respectively. After going through the two TL connected to P2, the existing two sidebands are then mixed with the LO signal for the second time with a phase at φ_{M2}, generating four frequency products, two of them located at ω_s with phase delays of $-2\varphi_0 - 2\varphi_1 - \varphi_{M1} + \varphi_{M2}$ and $-2\varphi_0 - 2\varphi_2 + \varphi_{M1} - \varphi_{M2}$. The phase delays of $-\varphi_0$, $-\varphi_1$ and $-\varphi_2$ result from spatial duplexing, whereas φ_{M1}, φ_{M2} and φ_{M3} result from the temporal modulation in each of the parametric mixers. The circulator can be designed in such a way that in the pass mode the two side bands at ω_s will be added in phase as shown in Fig. 3.4(a).

Likewise, in the isolation mode, the same RF signal starts at P1 and flows from P1 to P2 via P3. The RF signal is first multiplied with a LO signal at $\omega_m t + \varphi_{M3}$, resulting in two sidebands at $(\omega_s - \omega_m)\, t - \varphi_0 - \varphi_1 - \varphi_{M3}$ and $(\omega_s + \omega_m)\, t - \varphi_0 - \varphi_2 + \varphi_{M3}$. After passing through port P3 and experiencing the phase delays from the two TLs, the two sidebands are mixed with a LO signal for a second time generating four frequency products in total. The circulator can be designed in such a way that in the isolation mode the two side bands at ω_s will be added 180° out of phase, as shown in Fig. 3.4(b).

To achieve the ideal non-reciprocity at ω_s without conversion loss, the phase constrains on the TLs and modulators are given by (3.4)

$$\begin{cases} |cos\,(-\varphi_1 + \varphi_2 - \varphi_{M1} + \varphi_{M2})| = 1 & \text{(3.4a)} \\ cos\,(-\varphi_1 + \varphi_2 - \varphi_{M3} + \varphi_{M2}) = 0 & \text{(3.4b)} \end{cases}$$

where φ_1 represents the phase delay of the signal at $\omega_s - \omega_m$ through the TL segments, and φ_2 is the phase delay of the signal at $\omega_s + \omega_m$ and is larger than φ_1 through the TL media. Solving (3.4) one gives the conditions to obtain ideal nonreciprocal transmission.

One feasible solution is given in (3.4), where $\varphi_2 - \varphi_1 = 30°$.

$$\begin{cases} \varphi_2 - \varphi_1 = 30° \\ \varphi_{M1} = 330°(-30°) \\ \varphi_{M2} = 120° \\ \varphi_{M3} = 240° \end{cases} \tag{3.5}$$

Based on the above analysis it can be seen that the LO phases do not necessarily have to be set at 0°, 120° and 240° as employed in the existing circulator works [16, 19]. By setting the LO phases according to (3.5), the proposed circulator has an important advantage over the exiting works in that the frequency-dependent conversion loss which exists in the architecture in [16, 19], caused by the modulation scheme, can be eliminated. This leads to lower conversion loss in our proposed approach. The analytical results are verified by simulated and measurement result in Section 3.3.

The impedance matching requirements in the demonstrated spatio-temporal modulated circulator is not as stringent as in the conventional SIC (self-interference cancellation) antenna interface [27]. In the SIC circulator, any direct or indirect coupling between the two ports can detriment the isolation. However, in our presented circulator, the direct path from TX to RX is physically isolated with high impedance. The only fundamental components at ω_s present at the LNA port are the reconstructed ones which are controlled by the phase differences between the two fundamentals. Assuming the impedance is not perfectly matched at the LNA or ANT port, it may slightly affect φ_0 which would cause phase mismatch between φ_1 and φ_2 in (3.5). When the impendence mismatch is moderate (return losses $\geq$ 10dB), it can be compensated by tuning φ_1 and φ_2 by adjusting the modulation frequency or modulation power of the circulator with minor increase of TX-RX IL due to the phase mismatches of φ_1 and φ_2 after the compensations. Therefore a good isolation is basically determined by how well the two reconstructed components cancel out with each other at ω_s. Similar results in [16, 22] present moderate impedance matching yet high isolation as well.

3.1.2.3 Operation Principle Using Telegrapher's Equation Theory

The voltage of the signal travelling along the NTL can be analyzed using Telegrapher's equation assuming the variation of the capacitance is small and the transmission line is nondispersive over the band of interest [9, 25, 28]. The signal of tone ω_s will be passed entirely in one direction from the RF_in to RF_out, thus forming the pass mode for ω_s in this direction and meanwhile in the other direction (from RF_out to RF_in) the side bands of $\omega_s \pm 2\omega_m$ will be passed while signal of ω_s becomes zero, thus forming the isolation mode for ω_s.

In the pass mode, when the RF signal of frequency ω_s is injected from the RF_in port, the transmission property can be analyzed with the expression of S21 in [16,26]. The isolation between the RF_in and RF_out can be defined as

$$S21\left(\omega_s\right) = 1 - 3\left(\frac{sin\left(N\omega_s\Delta Z/v_p\right)}{Nsin\left(\omega_s\Delta Z/v_p\right)}\right)^2 \tag{3.6}$$

where N represents the number of mixing units, ΔZ is the length of TL section between two adjacent varactors, and v_p is the phase velocity of the RF signal. The square term in (3.6) contains a SINC function which reaches its first null, when $N\Delta Z$ approaches $\lambda_s/2$. This means that, under this condition, the energy of RF signal of ω_s is maintained through the isolator without being converted to any sidebands [26]. Consequently, in the pass mode, low insertion loss is achieved in broadband and the in-band loss of an isolator is the same as that of a regular TL.

Contrarily, in the isolation mode when the RF signal of frequency ω_s is injected from the RF_out port, the $S12$ at ω_s and the average power at side bands $P_{s\pm Nm}$ are as follows [26]:

$$S12\left(\omega_s\right) = \cos^2\left(\frac{1}{2\sqrt{2}}\xi\frac{\omega_s}{v_p}z\right) \tag{3.7}$$

$$P_{s\pm Nm}\left(z\right) = \frac{{V_0}^2}{4Z_0}\left(\frac{\omega_{s\pm Nm}}{\omega_s}\right)\sin^2\left(\frac{1}{2\sqrt{2}}\xi\frac{\omega_s}{v_p}z\right) \tag{3.8}$$

where v_p is the phase velocity of the RF signal, Z_0 is the characteristic impedance of the transmission line, and $\xi = {C'}_m/{C'}_0$, in which ${C'}_0$ and ${C'}_m$ represent the mean capacitance per

unit length and the capacitance variation per unit length, respectively. From (3.7) and (3.8), it can be observed that at a distance of $z = \lambda_s/\xi\sqrt{2}$, $S12(\omega_s)$ is 0 whereas the two sideband power is at maximum, which means that all the energy of the input tone ω_s is converted to the sidebands. This unique characteristic implies the isolation can reach infinitely high, a feature that conventional switches do not present. It is possible to choose a ξ and a TL length such that the same NTL will result in $S21(\omega_s) = 1$ in the pass mode and $S12(\omega_s) = 0$ (infinite isolation) in the isolation mode. Moreover, by choosing the modulation direction with respect to the RF signal direction, the isolation direction can be configured in either direction.

Different from the existing spatio-temporal modulated isolator in [9, 18, 25], there are three major highlights in the proposed isolator. First it operates in a single-ended method without having to employ a differential structure to reduce its RF feedthrough due to the non-isolated RF signal path. Second, it merges the LO modulation path into the RF path to produce the temporal modulated signals. These two features, along with the resonant-type modulation topology, make it possible to utilize only two modulation stages to provide enough isolation at mm-wave frequencies. Meanwhile, the serial resonance provides ideally zero resistance at resonance, minimizing insertion loss.

3.2 CMOS Circuit Design and Optimization

3.2.1 Conversion Loss Optimization for the Isolator

To implement the proposed isolator operating at 100 GHz in silicon, an on-chip N-POLY/NWELL varactor is adopted as capacitive-mixing components with specific capacitance of $10fF/\mu m^2$ and voltage coefficient of 0.95/V over 0 to 1V. On-chip TLs are utilized as inductors in parallel with the varactor to form the LC mixing stages.

In the pass mode of the isolator, according to (3.2a), if the two RF fundamentals produced by the spatio-temporal mixing stages are not exactly in phase, then (3.2a) will be evaluated less than 1. The loss due to this phase mismatch is defined as conversion loss. Similar to regular passive components, the intrinsic loss comes from the attenuation loss when the RF signal transmits along the TL structure. The conversion loss and intrinsic loss are the two main contributions to the insertion loss of the isolators.

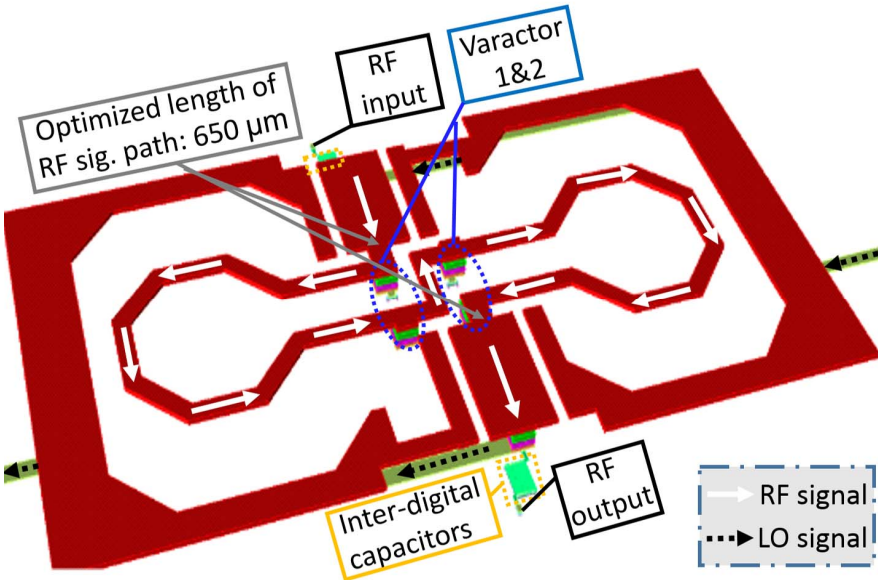


Figure 3.5: Passive layout of the isolator modulators for parameter optimization of the isolator.

There exist multiple solutions of φ_1, φ_2 and φ_M that would meet the conditions of equations (3.2), and when ω_s and ω_M are fixed, these multiple solutions imply that there exist multiple TL lengths that meet the requirements of (3.2). In practice, longer length introduces higher intrinsic loss, but the higher impedance of the LO signal path driven by LO signal source can help to reduce the modulation power. The selection of the TL length is determined by the tradeoff among intrinsic loss, conversion loss and modulation power.

The length of the TL path should be properly selected to ensure the conversion loss is almost zero according to (3.2a). Meanwhile, the intrinsic loss and modulation power have to be considered as well. EM simulations on the device level need to be performed to study the tradeoff among the modulation power, IL and conversion gain and to identify the optimal length for the minimal IL.

Fig. 3.5 shows the layout of the mixing stages. To simulate the conversion loss over the length of the RF signal path between the two varactors, the parameters of the passive structures are first extracted using EM simulation tools. Then the varactor capacitance is loaded to the passive structure. Fig. 3.6 records the simulation results of the intrinsic loss, the conversion loss and modulation power, all as a function of the length of the RF signal

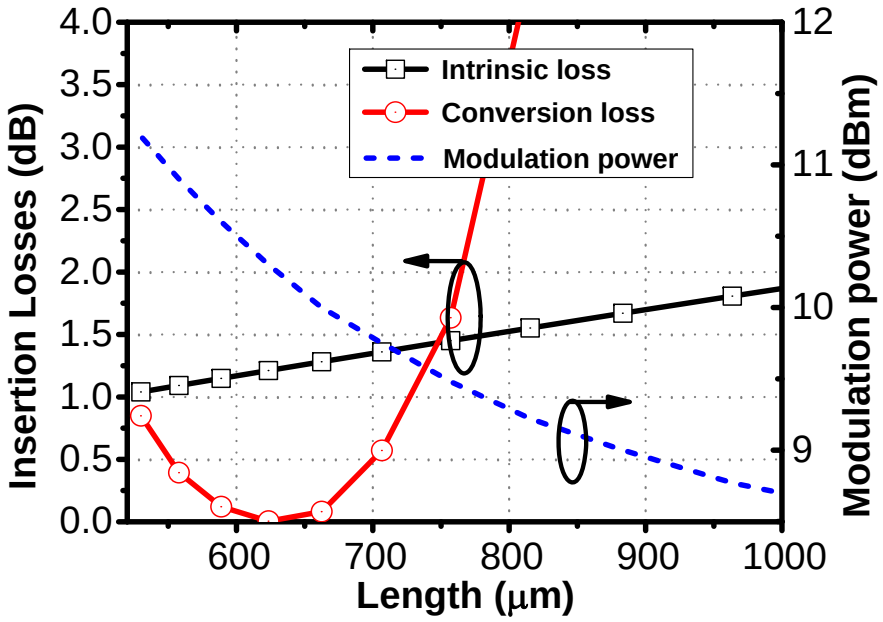


Figure 3.6: The modulation power and insertion losses over the length of the isolator at 100 GHz.

path. In this design, the modulation frequency is selected at 10 GHz and intrinsic loss of the isolator at 100 GHz. Metal inter-digital cap can be used as HPF for their low noise figure, high Q-factor, and high resonance frequency.

From Fig. 3.6, it can be observed that in the pass mode at 100 GHz, the conversion loss is below 0.5 dB from 550 μm to 700 μm, indicating that the insertion loss is mostly contributed from the intrinsic loss. Within the range of the low conversion loss, the modulation power decreases as the inductive loading increases with the length of the TL. By contrast, the IL increases when the RF path becomes longer. To trade off the modulation power, IL and conversion gain, the length of the RF signal path can be chosen to be 650 μm, thereby achieving moderate modulation power of 9.6 mW and insertion loss of 1.3 dB.

The transmission properties of the unmodulated isolator are simulated in terms of S-parameters in Fig. 3.7. It can be observed that the resonant type of matching is achieved when the series resonance occurs around 100GHz when the two parametric mixers resonating at 76 GHz and 160 GHz, respectively. The resonant type of matching is achieved to minimize the scale of the matching network and additional losses inside it. Under the DC biasing

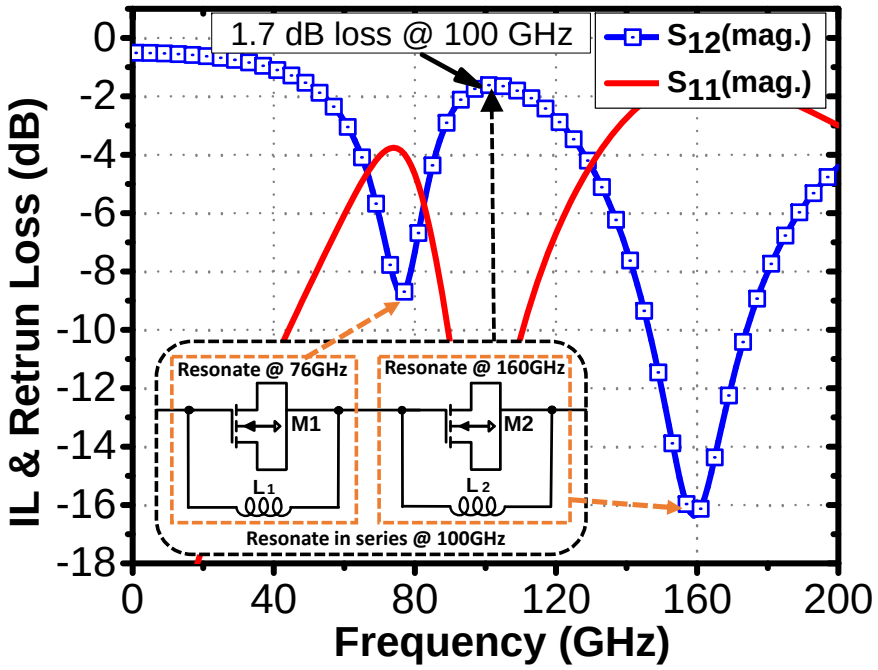


Figure 3.7: S-parameter simulation results of the isolator with two serially-resonate modulators.

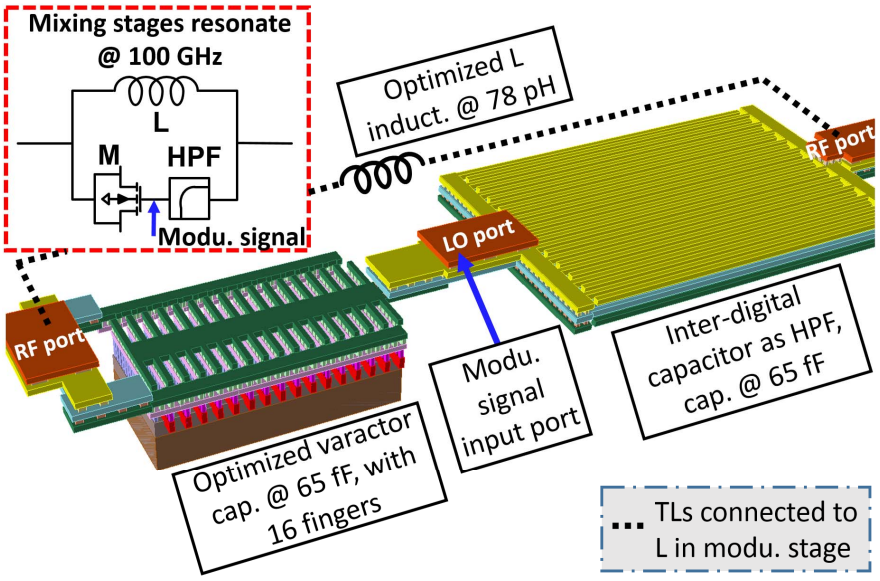


Figure 3.8: Layout of the parallel LC mixing stage for parameter optimization of the circulator.

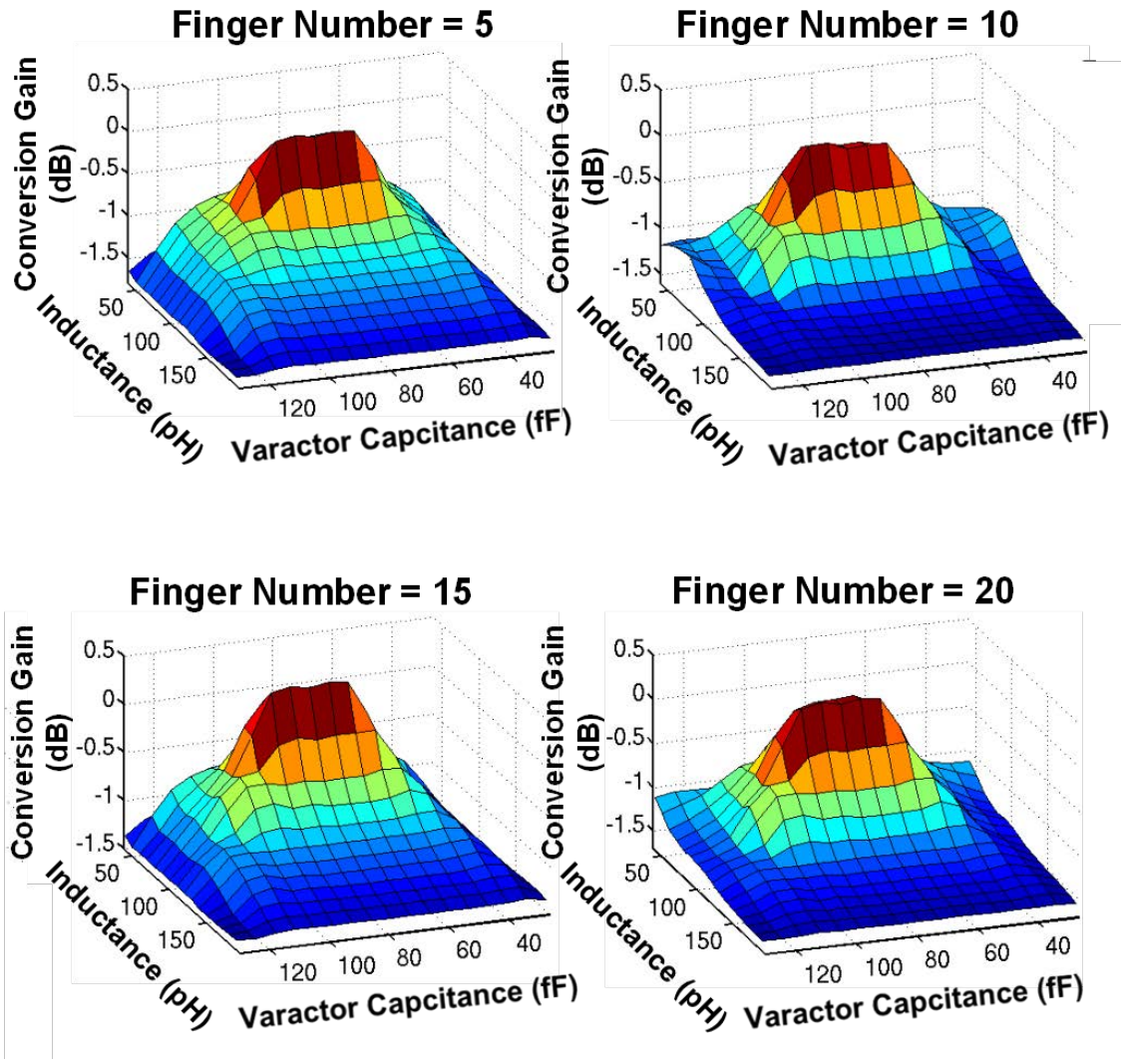


Figure 3.9: Mixing stage optimization of the circulator: the simulated conversion gain of the parallel LC modulator resonating at 100 GHz over the varactor capacitance and modulator inductance with different finger numbers of the varactor.

voltage of the LO signal at 0.5 V, the IL is 1.7 dB, which has the lowest intrinsic loss of the isolator at around 100 GHz.

3.2.2 Conversion Gain Optimization and Design Parameters

To implement the mixing stages in the circulator as described in Section 3.1, three identical varactors are chosen as capacitive-mixing components which are the same to the type used in the isolator. High Q-factor inter-digital capacitors are adopted as high-pass filter which has the same capacitance as the varactor and connected to the cathode node of it.

The modulation signal frequency is selected at 10 GHz. The IL at the RF signal frequency is determined by the conversion gain of the mixing stages.

Fig. 3.8 illustrates the layout of the varactor and high-pass filter in the mixing stage in CMOS process. The resonance frequency at 100 GHz constrains the product of inductance and capacitance of the mixing stage according to (3.3). For the parallel LC tank as a mixing stage, the modulated current I_M from the varactor is given by [29]

$$I_M = \Delta C_M \frac{d\left(V_M(t) \times V_s(t)\right)}{dt} \tag{3.9}$$

where $V_M(t)$ and $V_s(t)$ represent the modulation signal voltage and RF signal voltage respectively. ΔC_M is caused by $V_M(t)$ which is the capacitance variation propositional to varactor capacitance. When the inductance increase, the Q-factor of the mixing stage increases resulting in increased conversion gain. On the other hand, the modulated current from the varactor is decreased which will, in turn, degrade the conversion gain of the mixing stage. The mixing stage can be optimized by simulating its highest conversion gain over the different varactor capacitance and modulator inductance with different finger numbers as shown in Fig. 3.9.

From Fig. 3.9, it can be observed that the conversion gain experiences its peak values when the varactor capacitance value is from 60 fF to 90 fF and inductance value is around 80 pH. The conversion gain reflecting the total Q-factor of the mixing stage varies according to different inductance and varactor capacitance. The Q-factor of the mixer is also largely determined by the number of varactor fingers.

For the mixing stages in the circulator, the highest conversion gain of about 0.3 dB occurs when varactor capacitance is 65 fF, inductance value is 78 pH and the finger number of the varactor is 16. The conversion gain of the isolator mixing stages are optimized in the similar approach as well while satisfying the design principles in Section 3.1. The design parameters of the mixing stages in the proposed isolator and circulator are listed in Table 3.1. The Q-factors of the inductors and varactors vary across the RF band. The Q-factors of the LC tanks largely depends on the Q-factors of the varactors.

Table 3.1: Design Parameters of the Mixing Stages in the Isolator and Circulator

Type	Mixing stages	Ind. L (pH)	Q-factor (L) max/min	Vara. C (fF)	Q-factor (C) max/min	Q-factor (tank)
Isolator	Stage 1	50	34/31	86	18/15	12
	Stage 2	50		20	17/14	10
Circulator	Stage 1,2,3	78	34/32	65	17/16	11

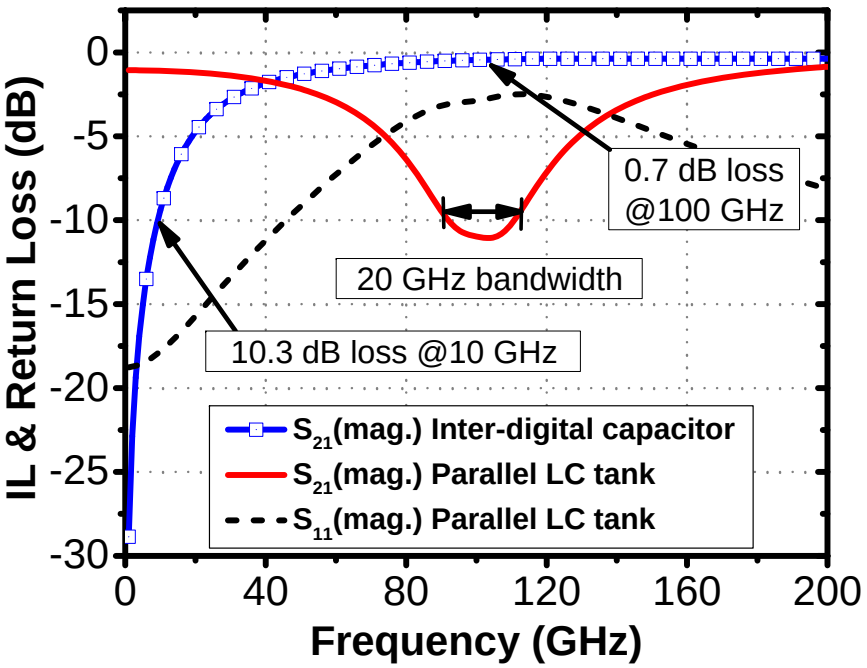


Figure 3.10: S-parameter simulation results of the band-stop filter using the parallel LC resonator and high-pass filter using the inter-digital capacitor.

3.2.3 High-pass Filter and Band-stop Filter Design

To prevent the RF signal from leaking through the LO modulation path, band-stop LC tanks resonating around 100 GHz are placed at the input and the output of the LO signal path, as shown in Fig. 3.1. By concatenating the two LC tanks with slightly different resonance frequencies (95 GHz and 105 GHz), wideband RF-to-LO leakage of -12 dB is achieved. The S-parameters from EM simulation are shown in Fig. 3.10. A wide blocking range of 28 GHz centered around 100 GHz is achieved with over 10 dB return loss.

To block the LO leakage, a high-pass filters (HPF) is proposed to be connected at the input and output of the RF path to prevent the modulation signal from leaking through the LC tank. Metal inter-digital capacitors are also used here. The S_{21} of the inter-digital capacitor is depicted in Fig. 3.10, which also shows a low IL of 0.7 dB that is experienced in the RF band, whereas LO-to-RF leakage of -10.3 dB is experienced in the LO band.

3.2.4 Hybrid Coupler Design for Nonreciprocal Transmission Line Based Circulator/Duplexer

Based on the two building blocks non-reciprocity TL and 90° hybrid coupler, the block diagram of the circulator and duplexer are shown in Fig. 3.11. The nonreciprocal TL can separate two inverse directional signals and the hybrid coupler can provide high isolation between TX and RX. Both circulator and duplexer operating at 100 GHz with 45 dB isolation and 9.5 dB insertion loss(IL).

As shown in Fig. 3.11, hybrid coupler is introduced to separate the TX signal path and RX signal path along the nonreciprocal TLs. Compared to the hybrid using lumped elements, the hybrid using $\lambda/4$ transmission lines can significantly reduce the mismatch at mm-wave frequencies from parasitic effects and increase the quality factor. Different from the conventional directly-coupled meander-line hybrid coupler, the proposed hybrid coupler have two TLs stacking up with strong capacitively and inductively coupling to greatly reduce the chip size as shown in Fig. 3.12(a) .

A compact transformer-based hybrid coupler is realized with the core area of 80×160 μm^2, as shown in Fig. 3.12(a). The quadrature hybrid coupler can be modeled by a coupled $\lambda/4$ T-line structure as shown in Fig. 3.12(b). When voltage V is excited at port 1, the output voltage at port 2 will be isolated, and output voltage at port 3 and port 4 can be

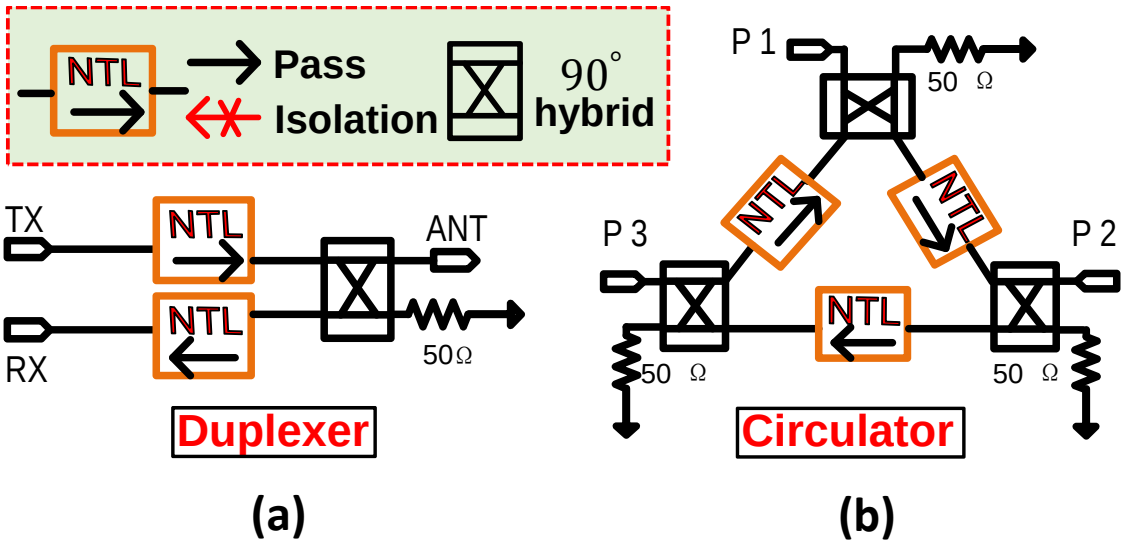


Figure 3.11: Block diagram of the proposed circulator/duplexer based on nonreciprocal transmission lines and 90° hybrid couplers

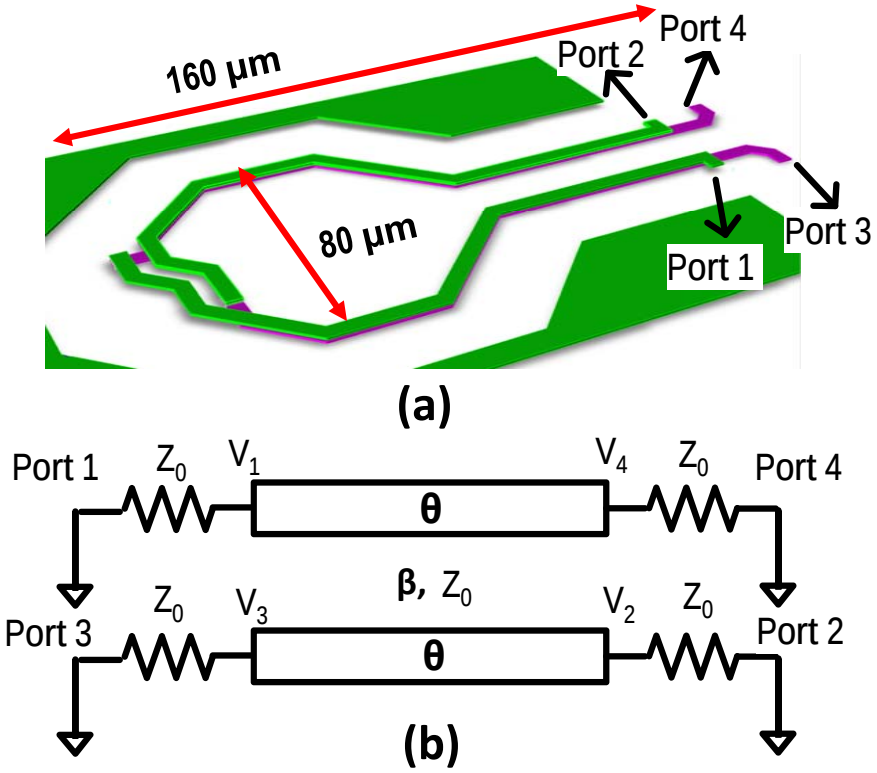


Figure 3.12: (a) Layout of the quadrature hybrid coupler. (b) Coupled TL model of quadrature hybrid coupler.

expressed as

$$\begin{cases} V_3 = V\dfrac{jc\tan\theta}{\sqrt{1-c^2}+j\tan\theta} & \text{(3.10a)} \\ V_4 = V\dfrac{\sqrt{1-c^2}}{\sqrt{1-c^2}\cos\theta+j\sin\theta} & \text{(3.10b)} \end{cases}$$

where c is the coupling factor which is a positive number between 0 and 1 to express the coupling effect between the two transmission lines. θ is the coupler length. Divide V_4 by V_3, one can get

$$\frac{V_4}{V_3} = \frac{\sqrt{1-c^2}}{jc\sin\theta}. \tag{3.11}$$

Equation (3.11) reveals that, regardless of the coupling factor c and coupler length θ, there are always 90° phase shifting between ports 3 and 4 inside the coupler. Meanwhile two coupling signal at port 2 have 180° phase difference and cancel out with each other achieving good isolation between port 1 and port 2.

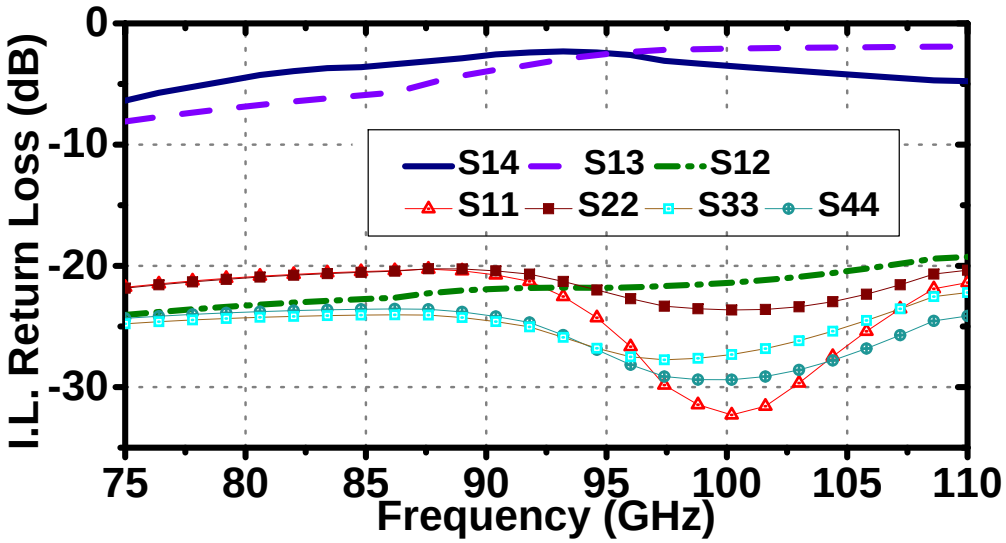


Figure 3.13: S-parameter simulation results of the hybrid coupler.

The EM simulation results of the proposed hybrid coupler are depicted in Fig. 3.13. It is shown that all ports of the coupler are matched to 50 Ω, and the TX/RX isolation between port 1 and port 2 is more than 20 dB from 75 to 105 GHz. The insertion loss from port 1 to port 3 and 4 are less than 4 dB at 100 GHz. The proposed compact hybrid coupler can be easily integrated with the nonreciprocal TL, which provides great isolation and low IL for the on-chip full-duplex communication.

3.3 Experimental Results

3.3.1 Implementation and Experimental Results of the Isolator

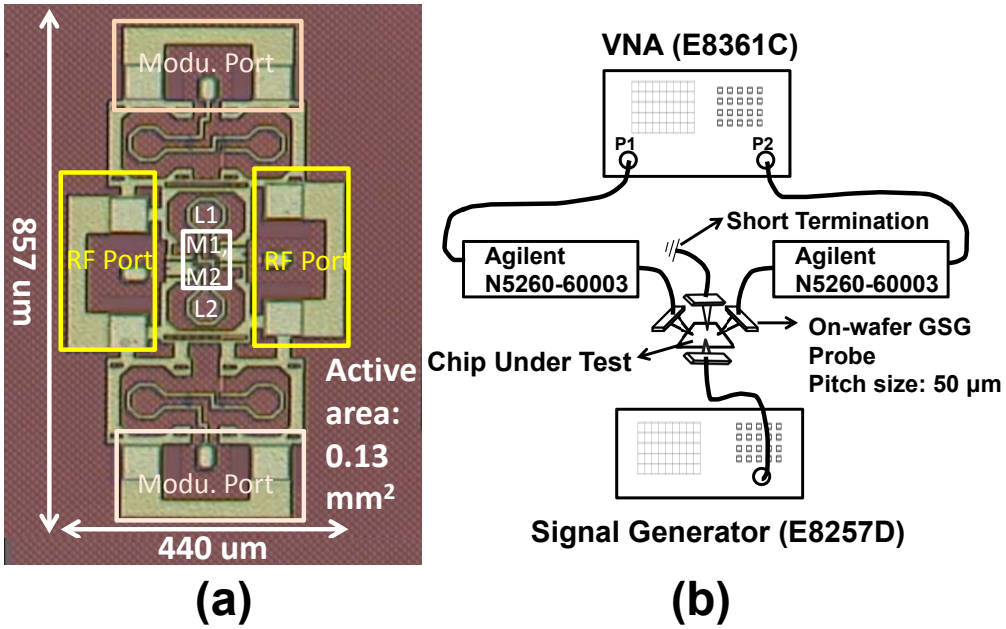


Figure 3.14: (a) Die photo of proposed isolator and (b) its S-parameter measurement setup.

The isolator is implemented in a standard bulk 65nm CMOS process. As shown in Fig. 3.14(a), the chip has an active area of 0.13 mm^2 without pads. The chip was characterized on a probe station (CASCADE WinCal Manual-1000) with a VNA (Agilent E8361C) and VNA extender (Agilent N5260-60003). The LO modulation signal was generated from a

signal generator (Agilent E8257D) and was injected into the chip through a probe, while the other probe at the LO output was short-terminated as shown in Fig. 3.14(b). The probes and cables were calibrated in SLOT method and RF pads were included in the measurement results.

The actual modulation frequency is measured at 17.4 GHz when the isolation is at the maximum according to (3.2). The reason for the shifted frequency between the measured and simulated modulation frequencies relates to inaccurates in the varactor device models.

The measured and simulated small-signal performance results show good agreement, as can be seen in Fig. 3.15. Non-reciprocity is simulated by combining a full-wave finite-element simulation of passive structures with a harmonic balance circuit simulation (ADS). Due to the measurement capability being limited to 110 GHz, the measured results only cover the pass-mode bandwidth of 25 GHz from 85 GHz to 110 GHz. The in-band return loss is more than 10 dB and the maximum insertion loss (IL) of 4.5 dB occurs around 97 GHz, while less than 6.5 dB IL was measured throughout the entire 85 GHz to 110 GHz range. At around 99 GHz, the isolation over a bandwidth of 1.5 GHz is as high as 45 dB, which agrees with our isolator operation principles described earlier.

As discussed in Section 3.1, the phase delays in (3.2) can be adjusted with different levels of varactor capacitance, therefore the isolation peak can be dynamically steered by changing the modulation voltage magnitudes. As illustrated in Fig. 3.16, the measured and simulated isolation peaks beyond 45 dB over 1.5 GHz bandwidth are observed at 90 GHz, 100 GHz and 105 GHz respectively, corresponding to three different modulation power levels. Note that the measured modulation power P_m here includes losses in the probes and connections along the LO signal path.

The measured and simulated large-signal performance is plotted in Fig. 3.17 at 85 GHz. During the measurement, the losses from probes and cables were calibrated and the measurement results agree well with simulation results until the input signal source reaches its maximum power. The simulation shows a 10.9 dBm input-referred 1-dB compression. The simulated noise figure (NF) of the isolator in the pass mode is 4.53 dB at 100 GHz.

A comparison to the state-of-the-art switches is presented in Table 3.2. The proposed isolator delivers over 15 dB higher isolation than the state-of-the-art switches and a band-

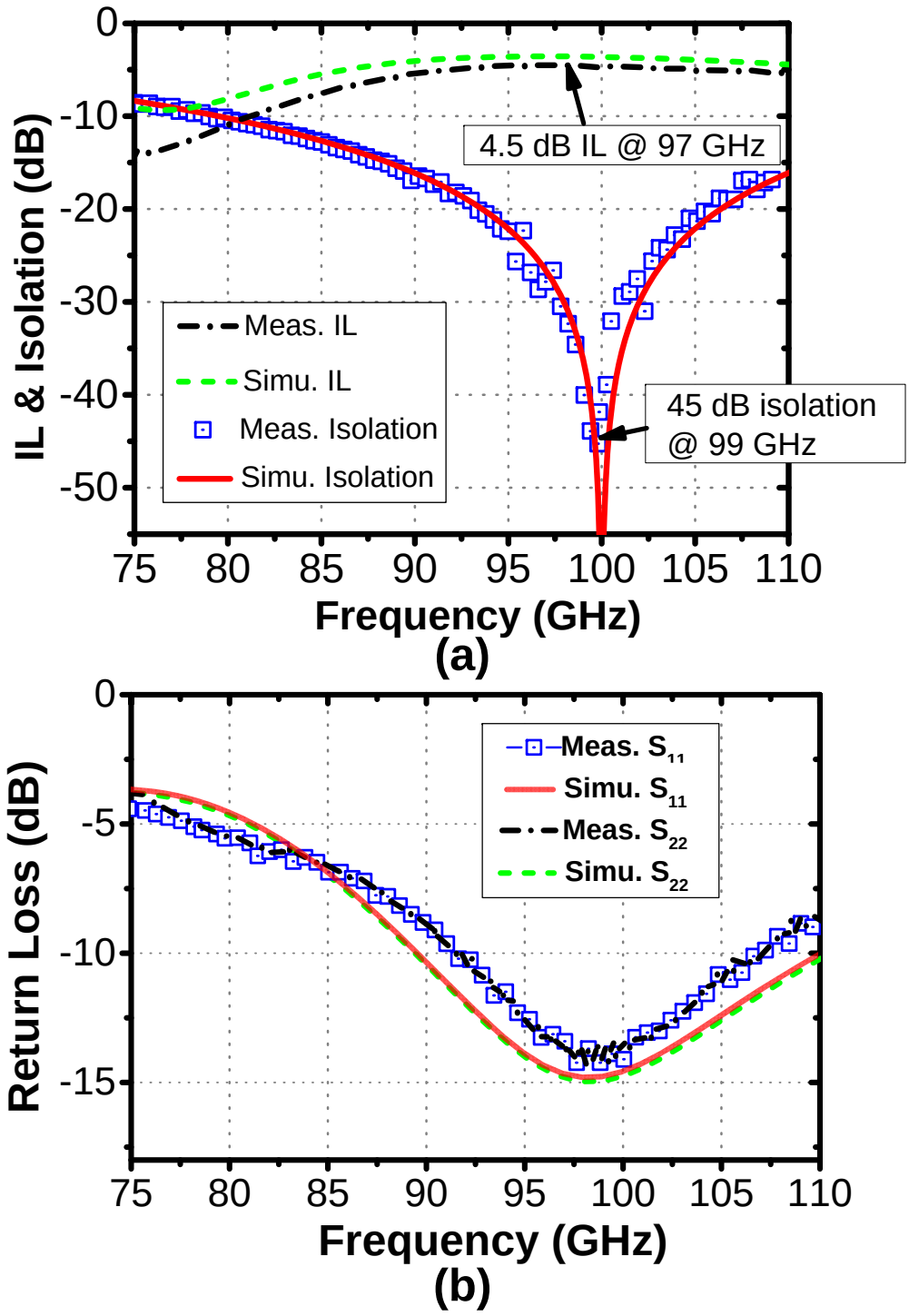


Figure 3.15: The measured and simulated (a) isolation, insertion loss (IL) performance and (b) return loss of the proposed isolator.

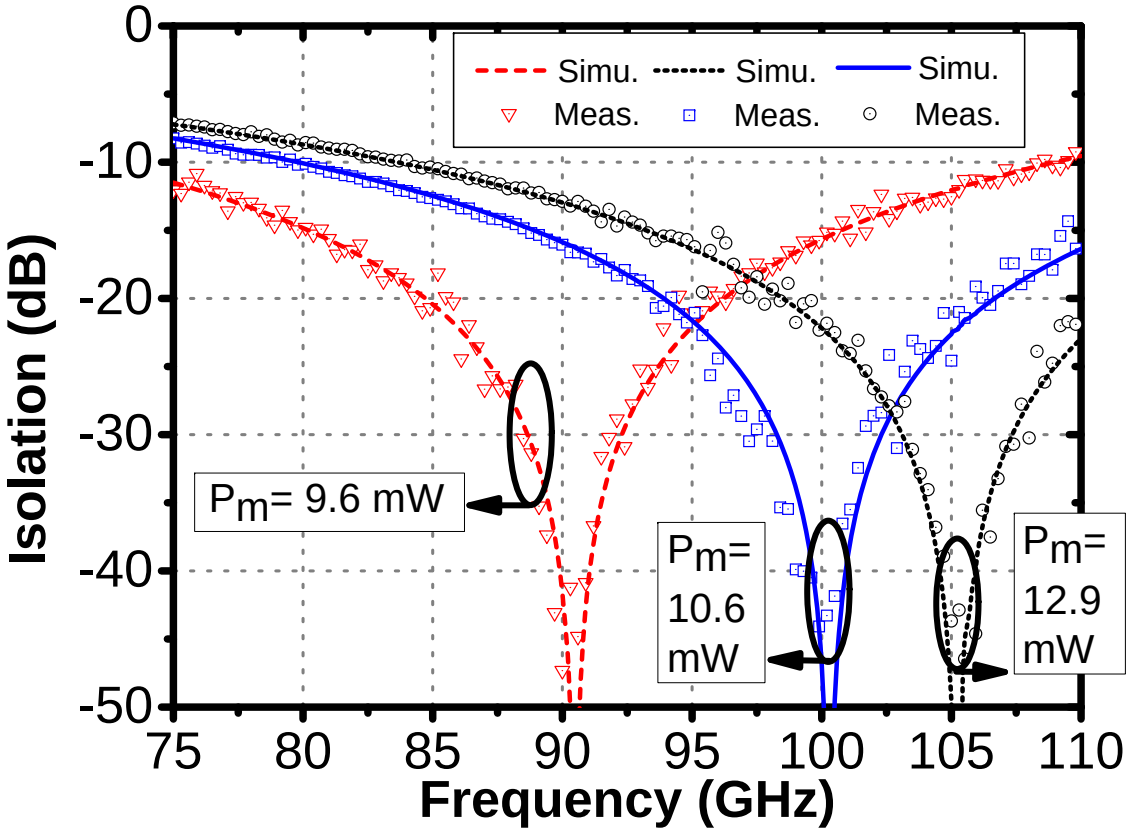


Figure 3.16: Measured and simulated isolation versus frequency for different values of modulation power P_m for the isolator.

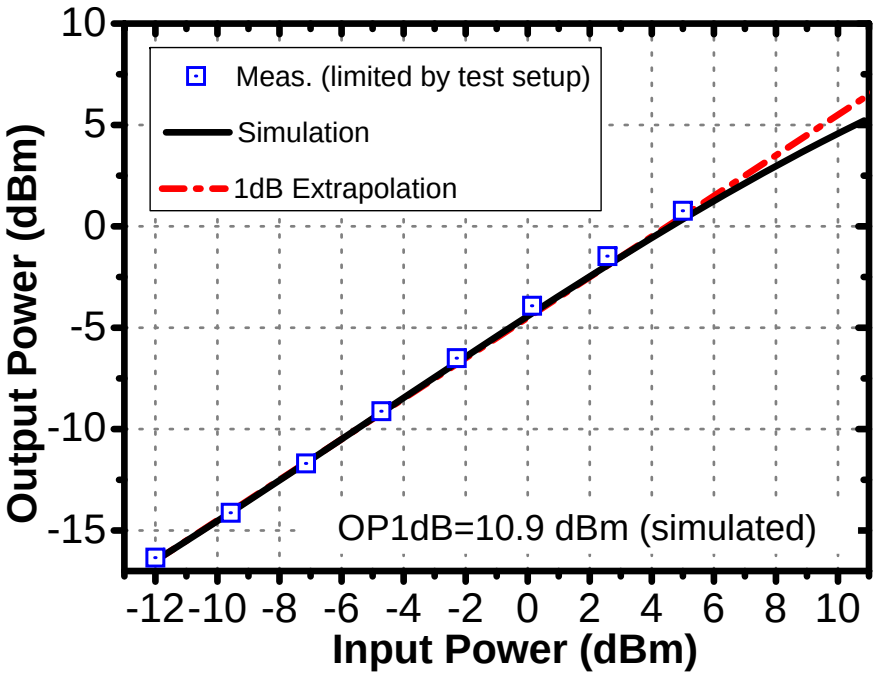


Figure 3.17: Measured and simulated large-signal performance of the isolator.

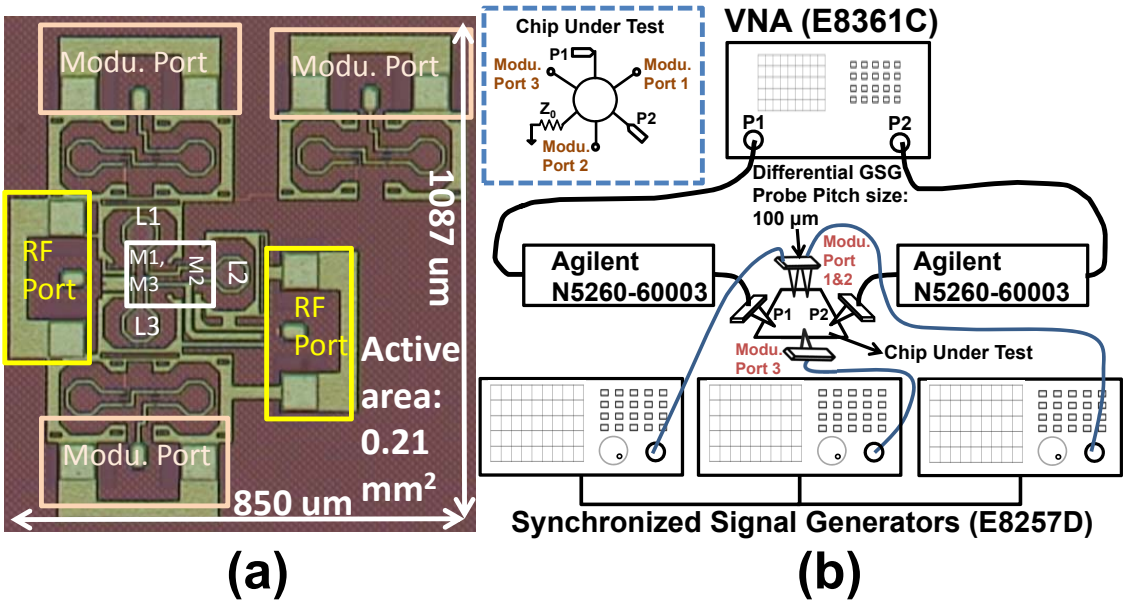


Figure 3.18: (a) Die photo of proposed circulator and (b) its S-parameter measurement setup.

width of 25 GHz in the pass mode, while maintaining a comparable IL. It can be used as reconfigurable isolator to route different MIMO transceiver channels in mm-wave communication [34–37].

3.3.2 Implementation and Experimental Results of the Circulator

The circulator is implemented in a standard bulk 65nm CMOS process. To choose the lengths of the TLs in Fig. 3.4, the lengthes of L_1, L_2 and L_3 in Fig. 3.3 are first determined according to (3.3). Then connected with the TLs, HPF and capacitors which to emulated the varactors the entire passive structure is run in EM simulation to meet $\varphi_2 - \varphi_1 = 30°$ in (3.5) by tuning the length of the TLs which is 196 μm. As shown in Fig. 3.18(a), the active chip area is 0.21 mm^2 without pads. The RF port P3 is terminated internally at Z_0 for simple measurement implementation. A 50 Ω poly-silicon resistor provided by the process is selected as termination. The parameters of the contacts and interconnections on the resistor are extracted by EM simulation then simulated together with the resistor models.

The measurement instruments are the same as those used in the isolator characterization. Three synchronized signal generators (Agilent E8257D) serve as modulation signal with required phase delays as shown in (3.5). A 'Thru' structure including RF pads and

interconnects is implemented on chip to calibrate the cable and parasitics which introduces additional phase shifting and losses to the LO signal paths. The measurement flow of the circulator is illustrated in Fig. 3.19. To get proper phase shift according to (3.5), the phase constant and attenuation constant of the interconnections are first extracted for calibration. Next, with the extracted parameters of the interconnections, a precise LO frequency are measured at 14.2 GHz to satisfy the $\varphi_2 - \varphi_1 = 30°$. Based on that, the maximum isolation occurs when the calibrated values of φ_{M2} and φ_{M3} are 120° and 240° respectively as shown in (3.5). Finally, an optimum φ_{M1} comes out when the circulator delivers the minimum IL without conversion losses.

According to (3.5), perfect nonreciprocity occurs when the measured isolation is at maximum meanwhile the measured IL is at the minimum, in other words, the conversion loss is 0. The calibrated actual phase of φ_{M1} is 325° (330° is the theoretical value according to (3.5)), which agrees well to the theoretical analysis. The 5° error here probably is introduced from asymmetric parasitics between the pass and isolation paths or errors in the cable calibrations. The measurement results verify the theoretical analysis on the circulator mixing with zero conversion loss in Section 3.1.

The measured and simulated small-signal performance results are shown in Fig. 3.20. The numerical simulation results are completed in both full-wave finite-element simulation for passive structures and ADS for the entire schematic.

For spatio-temporal modulated devices, the directions of the pass mode and isolation mode can be reconfigured by changing the circulation methods. When the perfect nonreciprocal conditions are satisfied, the circulation method can be switched by exchanging the modulation signal phases φ_{M1}, φ_{M2} and φ_{M3}. i.e. the clockwise circulation of the circulator is defined as the circulation method of $\varphi_{M1} = 240°$, $\varphi_{M2} = 120°$ and $\varphi_{M3} = -30°$. The counter-clockwise circulation is defined as $\varphi_{M1} = -30°$, $\varphi_{M2} = 120°$ and $\varphi_{M3} = 240°$. After switching circulation method, the transmission property between TX port and RX port of the circulator (S_{12} and S_{21}) will be exchanged.

The measurement results of the clockwise circulator are shown in Fig. 3.20(a). The measured results from 85 GHz to 110 GHz present the in-band return loss is over 10 dB and the maximum insertion loss (IL) of 5.6 dB at around 95 GHz, while less than 7.5 dB IL was

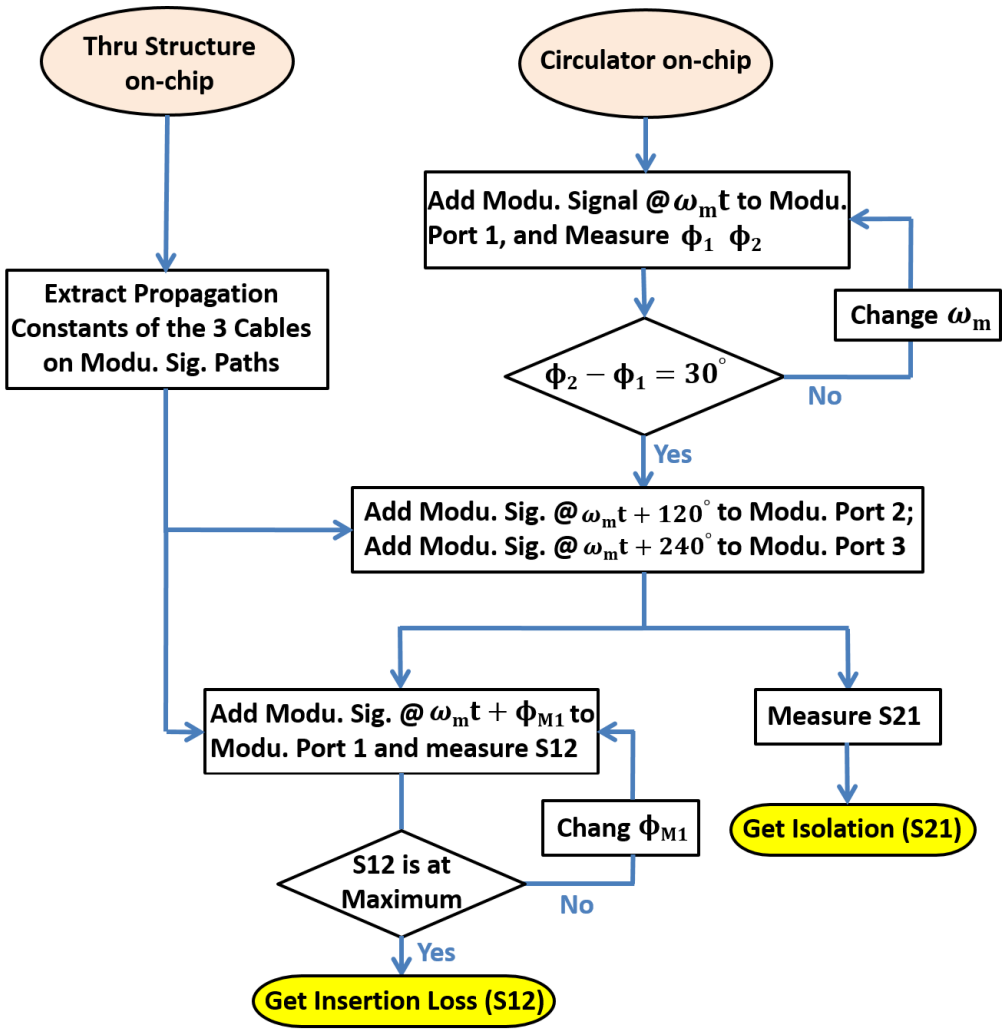


Figure 3.19: Measurement flow of the circulator for the maximum isolation and the minimum insertion loss.

measured across the entire 85 GHz to 110 GHz band. The isolation over a bandwidth of 1.5 GHz is around 47 dB at around 100 GHz, which is similar to the measurement results of the isolator. Similarly, the measurement results of the counter-clockwise circulator in Fig. 3.20(b) present the minimum IL of 5.6 dB at 95 GHz and the maximum isolation is 47 dB occurring at 99 GHz, meanwhile the directions of the pass mode and isolation mode are reversed. The return losses are identical for both clockwise and counter-clockwise circulator resulting from the sympatric topology.

Similar to the isolator, the isolation peak can also be steered with different modulation power levels. As depicted in Fig. 3.21, the measured and simulated isolation peaks beyond 45 dB are measured at 90 GHz, 100 GHz and 105 GHz corresponding to three different modulation power levels of the LO signal. For this circulator, the LO signal paths show high impedance with pure capacitance resulting in less than 3.63 mW power dispassion. The simulated power consumption of the three-phase LO paths for the proposed circulator is around 15 mW.

The measured and simulated large-signal performance is shown in Fig. 3.22 at 85 GHz for both clockwise and counter-clockwise circulation. After the effects of probes and cables are being calibrated, the measurement results show that in both operational modes, the measured P1dB values agree well with simulation results. After reaching the maximum power of input signal source, the P1dB is obtained from simulation results at 11.2 dBm for both operational modes of the circulator. The simulated noise figure (NF) of the proposed circulator is at 5.7 dB at 100 GHz which is close to the its IL. When the RF signal power becomes significant($>$ 4 dBm), the isolation bands of the isolator and circulator shift to lower frequency due to the modulation effect which is similar to the results in Fig. 3.16 and Fig. 3.21. According to our measurement results, changing the power of LO signal can compensate the isolation shifting when the single-tone RF signal (VIRGINIA Diodes WR10) is around 100GHz.

3.3.3 Experimental Results of Circulator/Duplexer based on Nonreciprocal Transmission Line

The simulated small-signal performance of the duplexer and circulator is depicted in Fig. 3.23. Non-reciprocity is simulated by combining a full-wave finite-element simulation

of passive structures with a harmonic balance circuit simulation (ADS) in which the 65nm CMOS substrate is fully modeled. NPOLY/NWELL varactor is adopted with specific capacitance at 10 fF/um^2 and voltage coefficient of $0.95/V$ over 0 to 1V. The isolation bandwidth is about 1.5 GHz. The in-band return loss is <-10 dB and the minimum insertion loss (IL) of 9.5 dB occurs at around 95 GHz. Meanwhile at the same region, the isolation is as high as 45 dB, realizing nonreciprocal transmission. The simulated 1dB compression point is at 9.5 dBm.

A comparison with published on-chip nonreciprocal components based on spatio-temporal modulation is presented in Table 3.3. The proposed circulator/duplexer delivers the maximum isolation of 45 dB, which is comparable that of the state-of-the-arts, a isolation bandwidth of 1.5 GHz, meanwhile a comparable P1dB result.

3.3.4 Comparison and Discussion

According to (3.2b) and (3.4b), any offsets from the ideal φ_1, φ_2 and φ_M will degrade the isolations of the nonreciprocal components which can be observed by measuring the isolations for different modulation frequencies as shown in Fig. 3.24. The measurement setups are consistent with what described in Section 3.3. The results reveal that, at 17.4 GHz and 14.2 GHz, isolation is perfectly achieved in the isolator and circulator, respectively. When the modulation frequency shifts, the conditions of isolation for (3.2b) and (3.4b) are not satisfied resulting in isolation degradation. At 12 GHz or 22 GHz, the isolations of the isolator only reached at 8.5 dB. Similarly, at 7 GHz or 21 GHz, the isolation of the circulator only became 11 dB and the LO bandwidth of the isolator is narrower than that of the circulator due to their different structures.

Fig. 3.25 shows the simulated harmonic spectrum at the output ports of the demonstrated nonreciprocal components. At the fundamental frequency of 100 GHz, the received signals at the pass mode and the isolation mode are consistent with the measured S-parameters which reflect the nonreciprocal transmission property. Fig. 3.25(a) is on the circulator case when the RF signal at 100 GHz and 0 dBm is injected from the TX port. Intermodulation (IM) frequencies at $\omega_s \pm n\omega_M$ are generated at the ANT and RX port. Similar to the results in [16, 20], most of the sideband energy is converted into the fundamental component. The

IM products are at least 16 dB smaller than the fundamental signal level. With the same RF input, Fig. 3.25(b) illustrates the harmonic spectrum at the receiving end of the isolator when the isolator operates at the pass mode and isolation mode. The IM products are 18 dB smaller than the fundamental signal level. The IM signal levels are safe enough to protect the RXs.

Compared to the state-of-the-art on-chip nonreciprocal components based on spatio-temporal modulation technique, the performance and features of the proposed two designs are listed in Table 3.4. The proposed isolator and circulator operate at the highest frequency at around 100 GHz with excellent isolation and tunable bandwidth than that of the state-of-the-art designs. The insertion loss and power consumption are balanced to compensate the high attenuation loss at 100 GHz. The low-side modulation scheme is more feasible in mm-wave regime. The structures are reconfigurable, robust and easy to be implemented with small chip footprints for the full-duplex transceivers with higher TX-RX isolation.

Table 3.2: Performance Summary and Comparison among On-chip State-of-the-art Works

	[30] JSSC 2010	[31] RFIC 2015	[32] JSSC 2012	[33] ISSCC 2015	Proposed Isolator
Topology	SPDT	SPST	SPST	Switchable Resonator	Spatio-temporal Modu.
Frequency (GHz)	102	69	93	155	100
Isolation BW (GHz)	16	30	35	50	1.5 †
Max IL (dB)	5	4	3.1 #	4	4.5
R.L. (dB)	>10	>10	>10	>10	>10
Isolation (dB)	25-30	35-40	21-22	21.1-23.7	45-46.5
P1dB (dBm)	N/A	10.5	N/A	11.4 *	10.9 *
Active area (mm^2)	N/A	0.012	10.5 §	0.0035	0.13
Tech.	65 nm CMOS	65 nm CMOS	0.18 μm SiGe	65 nm CMOS	65 nm CMOS

Pad loss deembedded * Simulation results † Tunable over 85-110 GHz
§ Include LNA+Mixer+IF Amp.

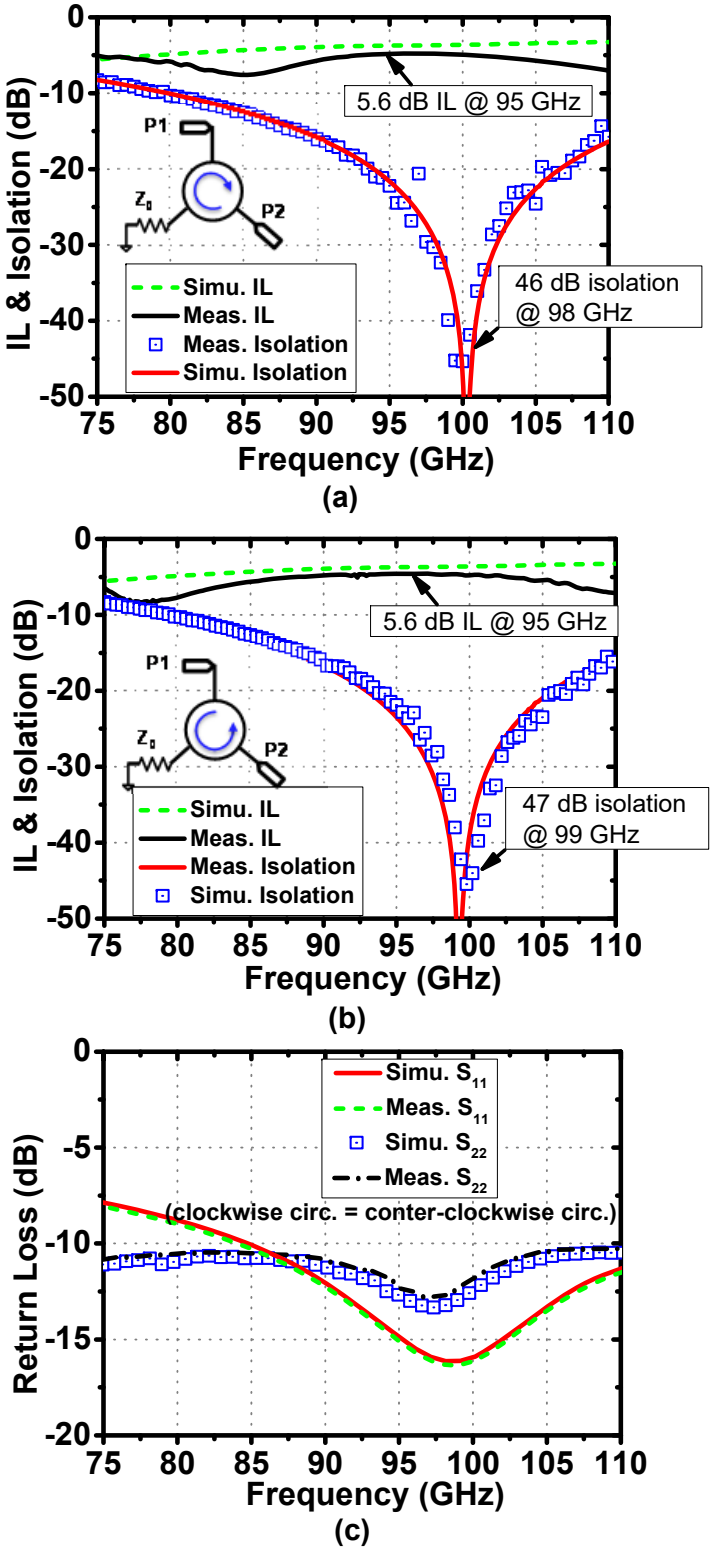


Figure 3.20: Measured and simulated results of isolation, insertion loss (IL) performance of the proposed circulator in (a) the clockwise circulation and (b) counter-clockwise circulation, (c) return loss from measurement and simulation results for the both modes.

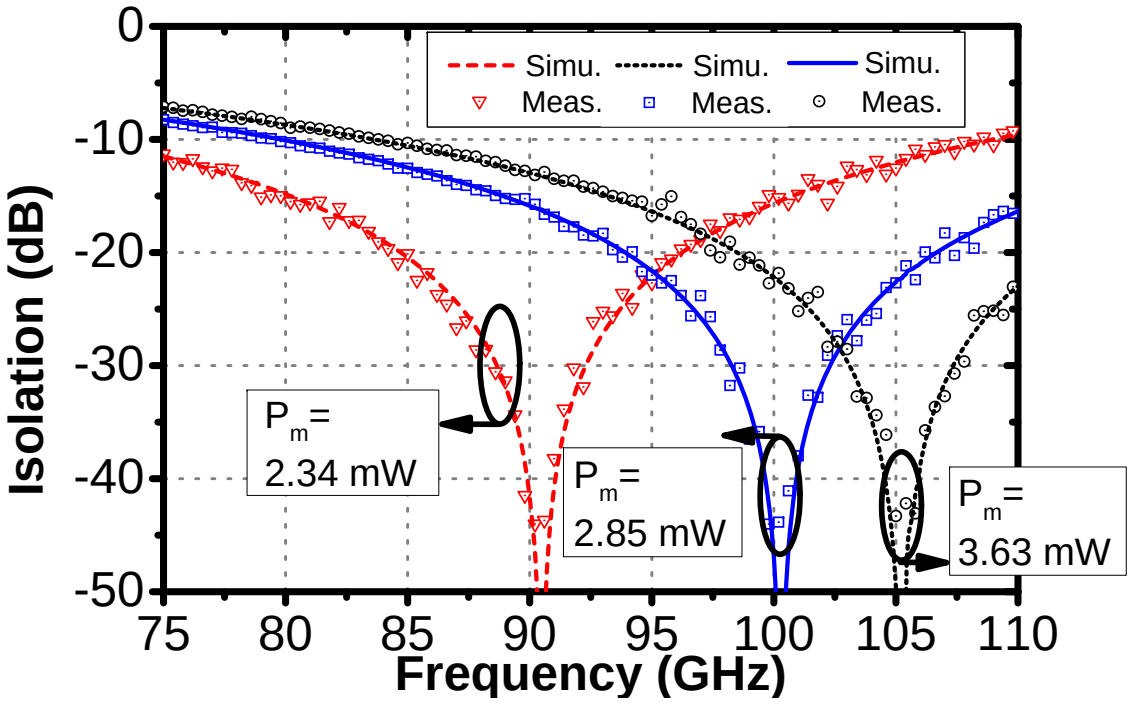


Figure 3.21: Measured and simulated isolation versus frequency for different values of modulation signal voltage P_m for the circulator.

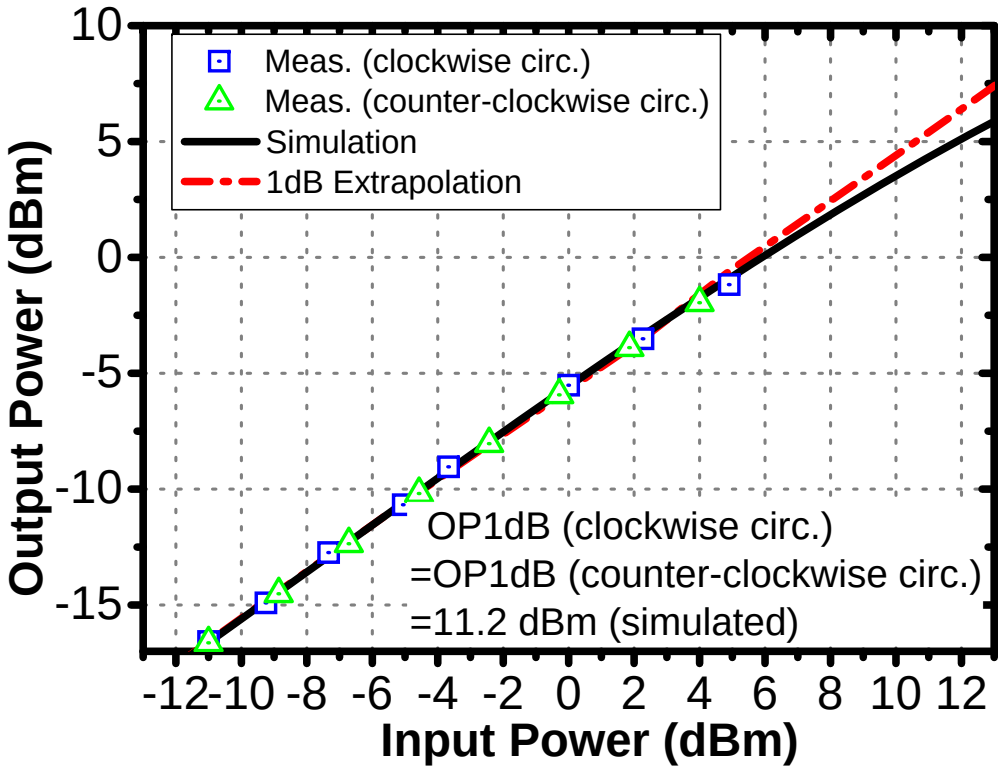


Figure 3.22: Measured and simulated large-signal performance of the circulator.

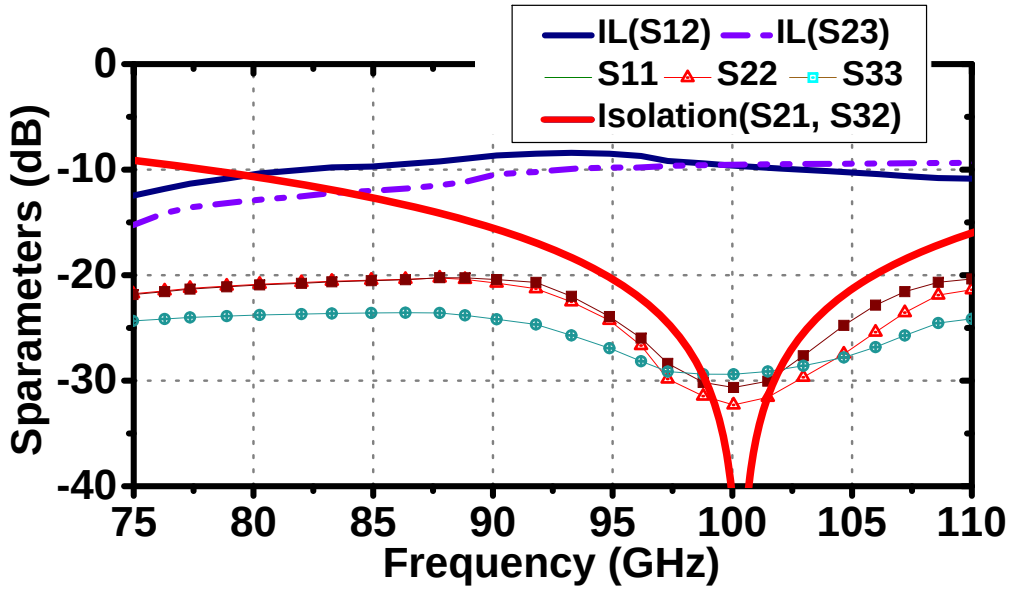


Figure 3.23: Isolation, insertion loss (IL) and return loss performance of the proposed duplexer/circulator from simulation results

Table 3.3: Performance Summary and Comparison among Nonreciprocal Transmission Line Based Circulator/Duplexer

	ISSCC 2017 [21]	JSSC 2017 [17]	IMS 2016 [9]	ISSCC 2017 [22]	This Work *
Topology	Circulator	Circulator	Isolator	Circulator	Duplexer Circulator
Band (GHz)	0.6-0.8	0.6-0.8	0.7-2.5	18.3-21.2	85-105
Min IL(dB)	1.7	1.7	-1 #	3.3	9.5
R.L. (dB)	<-10	<-10	<-10	<-10	<-10
Iso. (dB)	40	42	>25	18.3-21.2	45
Iso. BW (GHz)	0.2	0.2	1.8	2.9	1.5
P1dB (dBm)	N/A	N/A	10.5	21.5	10.9
Tech.	65 nm CMOS	65 nm CMOS	0.1 um GaN	45 nm SOI	65 nm CMOS

Pad loss deembedded * Simulation results

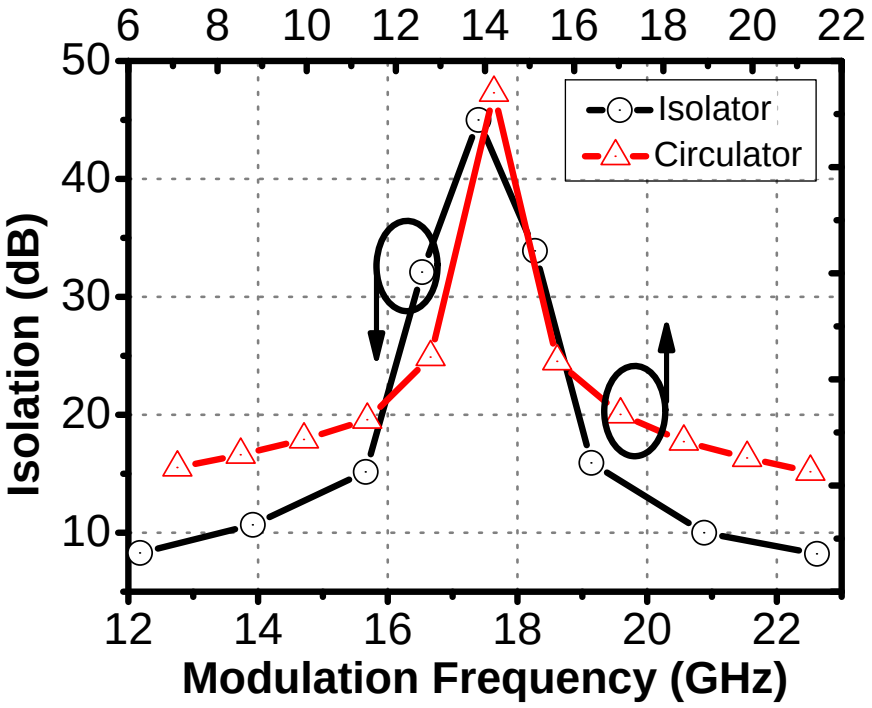


Figure 3.24: Measured isolation over modulation frequencies for the isolator and circulator.

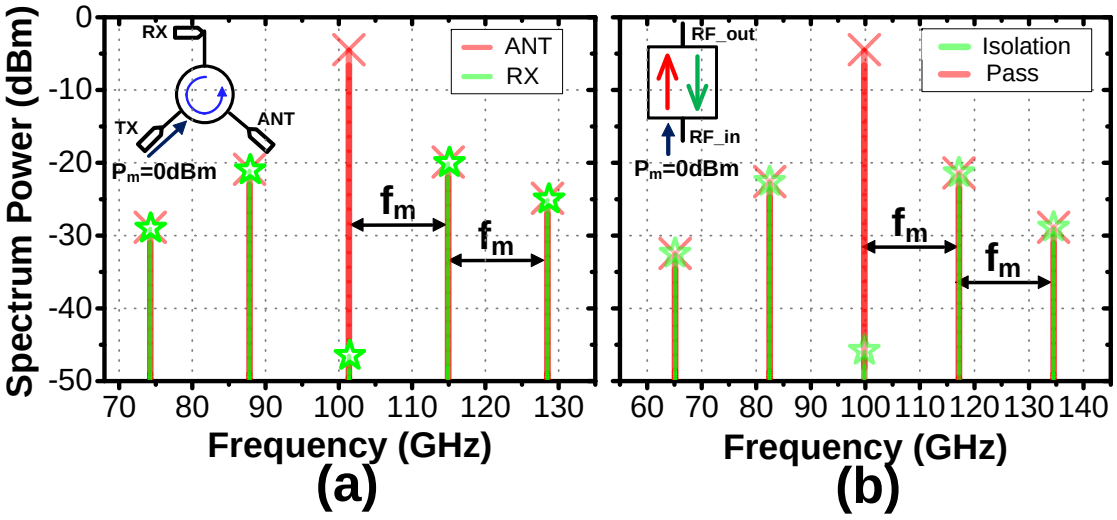


Figure 3.25: Simulated harmonic spectrum at pass and isolation mode for a signal tone input at 100GHz and 0 dBm (a) circulator. (b) isolator.

Table 3.4: Performance Summary and Comparison among on-chip Magnetic-free Nonreciprocal Components

	[21] ISSCC 2017	[17] JSSC 2017	[9] IMS 2016	[22] ISSCC 2017	This Work #1	This Work #2
Type	Circulator	Circulator	Isolator ⋆	Circulator	Isolator	Circulator
Topology	Staggered Commutated Network	Staggered Commutated Network	Shunt Modulated Capacitors	Conductance Mixing	Serially Resonated Modulators	Delta Resonators
Frequency (GHz)	0.7	0.7	1.6	25	100	100
Isolation BW (GHz)	0.2	0.2	1.8	4.5	1.5 †	1.5 †
Modu. scheme & LO band	High Side 2.8 GHz	High Side 0.75 GHz	High Side 6 GHz	Low Side 8.33 GHz	Low Side 17.4 GHz	Low Side 14.2 GHz
Insertion loss (dB)	1.8	1.7	2	3.2	4.5	5.6
R.L. (dB)	>10	>10	>10	>10	>10	>10
Isolation (dB)	40 ‡	>20 ♡	>25	18.3-21.2	45-46.5	46-47
P1dB (dBm)	N/A	N/A	10.5	21.5	10.9 *	11.4 *
NF (dB)	2-4♯	4.3	N/A	3.3	4.53 *	5.7 *
DC power (mW)	36	59	5.4 ♢	78.4	9.6-12.9	2.34-3.63+15 §
Tech.	65 nm CMOS	65 nm CMOS	0.1 μm GaN	45 nm SOI CMOS	65 nm CMOS	65 nm CMOS
Active area (mm^2)	0.94	0.64	11.76 ♢	2.16	0.13	0.21 ♢

‡ Across 20 MHz BW ♢ LO path not integrated on chip * Simulation results (limited by meas. facilities)
⋆ Circulator implemented by two identical isolators § Simulated power of LO paths is 15 mW
† Tunable over 85-110 GHz ♡ Across 12 MHz BW ♯ Depends on the balance impedance setting

Chapter 4

Motivation for On-Chip Gaussian Switching Regulation and Research Contribution

4.1 Background and Existing Work of Gaussian Switching Regulation for EMI Reduction

Several techniques have been reported to mitigate EMI. Passive input filters can reduce EMI but increase the system size and cost. Frequency stepping/dithering is proposed in [38–41]. While it is capable of deconcentrating the spur spectrum throughout the entire bands, in fact the modulated spur power density remains quite high especially in the high-frequency band. Using a resistor in series with the gate of the high-side switch (shown as M_H in Fig. 4.2) is another effective way to reduce EMI but permanently increase the switching time and conduction loss of M_H [42]. Additionally, multi-level driving strength is proposed to reduce the unwanted overshooting on the trapezoidal V_{SW}. As shown in Fig. 4.1, driving strength changes from low to high to turn on the high side switch M_H. Before the Miller plateau, the driving strength is low which results a low current slew rate of I_{DSH}, once Miller plateau is reached, the driving strength level is leveled up to get a high slew rate of the V_{DSH}. Before the Miller plateau, the approach reduces the EMI noise but compromises with power losses [40, 43], and moreover it becomes increasingly difficult to sense the starting point of the Miller plateau in a few nanosecond (ns) as f_{SW} goes up. In addition, the overshootings at V_{SW} due to the parasitics associated with M_H is only a partial source of EMI.

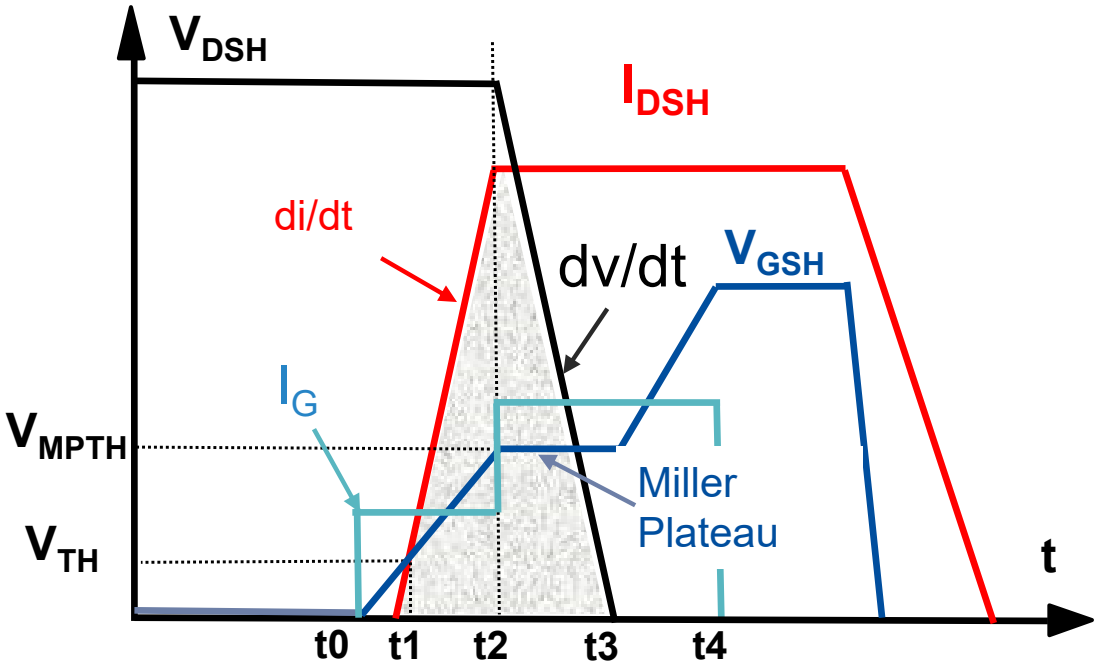


Figure 4.1: Key waveforms and corresponding power loss (in gray shade) of the buck converter with multi-level driving strength scheme to reduce the EMI noise.

As a novel approach to remove the high-order harmonics in V_{SW}, system-level study on the effects of Gaussian switching on switching power converters are presented in [44–46]. Fig. 4.2(a) and (b) provide a comparison on the switching node waveform and spectrum between the conventional trapezoidal switching and the Gaussian switching over GaN power switches. Externally implemented driving signal is exerted at the gate of the power switches to regulate the voltage across the power switches (V_{ds}) to track a Gaussian trajectory. Compared to the conventional trapezoidal V_{SW}, Gaussian V_{SW} can theoretically remove all the EMI harmonics above the Gaussian pole in the spectrum. To realize the Gaussian switching regulation, a feedback loop comprising of a Gaussian reference is implemented on the PCB-level operating at f_{SW} of less than 1MHz in [44–46]. Embedded into the control loop, these Gaussian references are realized in the FPGA or using passive Gaussian filters driven by a square wave source, which are bulky and unable to be integrated on chip. To track the Gaussian reference, an error amplifier or an ADC-based feedback loop [46] is commonly utilized which increases the complexity and power loss of the system. Moreover, while it is effective in

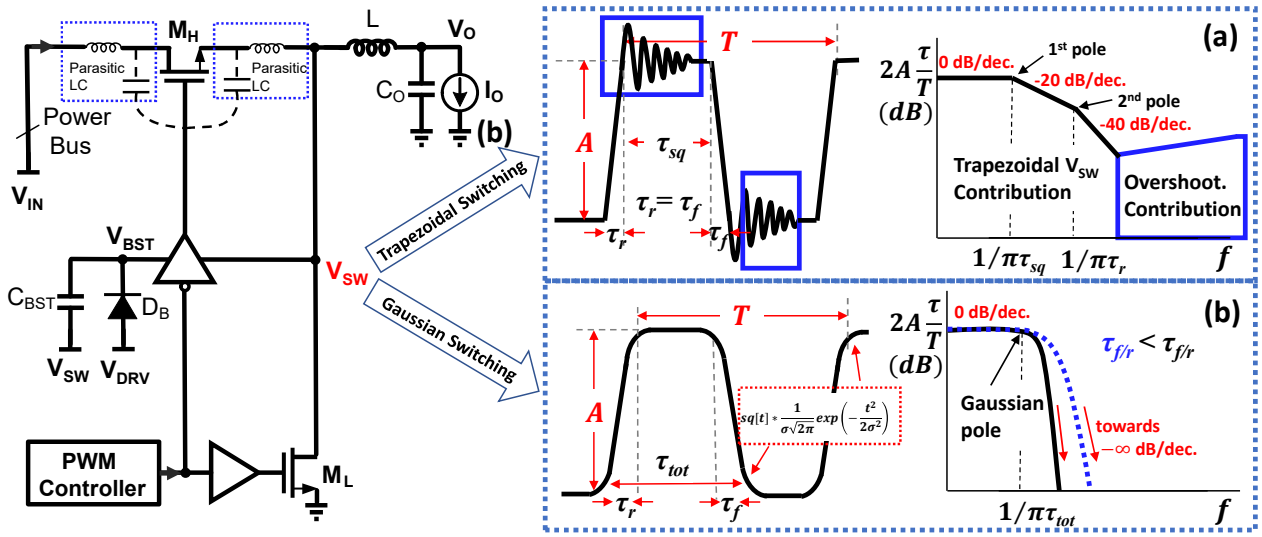


Figure 4.2: A typical power converter structure and the switching waveform and output spectrum of a power converter using (a) realistic trapezoidal switching waveform and (b) using the proposed gaussian switching waveform.

reducing EMI above its only pole, the Gaussian regulation is unable to reduce the EMI level in the frequencies below the pole. To deal with CISPR-25 EMC standard which covers a wide frequency range from 150 KHz to 108 MHz for conducted EMI noise [47], a comprehensive approach is needed at the circuit level to minimize the EMI throughout the entire bands.

4.2 Original Contribution

In this dissertation, a DC-DC converter with on-chip Gaussian switching regulation driving GaN power switches is presented to greatly reduce EMI noise in the high-frequency domain. Meanwhile, a spread-spectrum frequency dithering (SSFD) technique is proposed which is able to compress and evenly distribute several low-frequency harmonics below the Gaussian pole. The Gaussian regulation operates in a feed-forward way without using feedback loops or error amplifiers/ADCs so that it can be easily integrated on chip and operates at high switching frequency f_{SW}. To optimize the power efficiency, the presented Gaussian regulation scheme is designed with reconfigurable slew rate so that the power loss can be reduced to the minimum while satisfying the required EMI standard.

Chapter 5

Proposed GaN Gate Driver Using On-Chip Gaussian Switching Regulation

5.1 Gaussian Switching and Spread-Spectrum Frequency Dithering on GaN Power Switches

5.1.1 Gaussian Switching Characterizations

The signal switching characteristic at the switching node of a buck converter is one of the main factors determining its EMI and power efficiency [48]. In conventional buck converters, trapezoidal switching is employed with certain rise time τ_r, fall time τ_f and pulse width of τ_{sq}. The parameters τ_{sq} and $\tau_r(\tau_f)$ determine the location of the first pole and the second pole in the signal spectrum, respectively. The trapezoidal waveform can be constructed by convoluting a square wave $sq(t)$ with a short square pulse $g(t)$ waveform [49].

Similarly, Gaussian switching waveform is defined as the convolution of a square wave $sq(t)$ with the pulse width of t_{sq} and a normalized Gaussian function $\lambda(t)$ with the pulse width of t_g as shown in Fig. 5.1(a). The Gaussian switching signal can be expressed in time domain as

$$sw(t) = sq(t) * \lambda(t) = sq(t) * \frac{e^{-\frac{t^2}{2\sigma^2}}}{\sigma\sqrt{2\pi}} = sq(t) * \left[\frac{1}{A_{sq}}\frac{dr(t)}{dt}\right] \tag{5.1}$$

where σ is the standard deviation of the Gaussian function which equals $t_g/4$ [45], A_{sq} is the amplitude of the square wave $sq(t)$ and $r(t)$ represents the falling/rising edge portions of the generated Gaussian switching signal $sw(t)$ as shown in Fig. 5.1(b). The normalized Gaussian function $\lambda(t)$ is the derivative of the transient function $r(t)$ (falling/rising portion of $sw(t)$) divided by its amplitude A_{sq} as represented in Fig. 5.1(b) [44, 49].

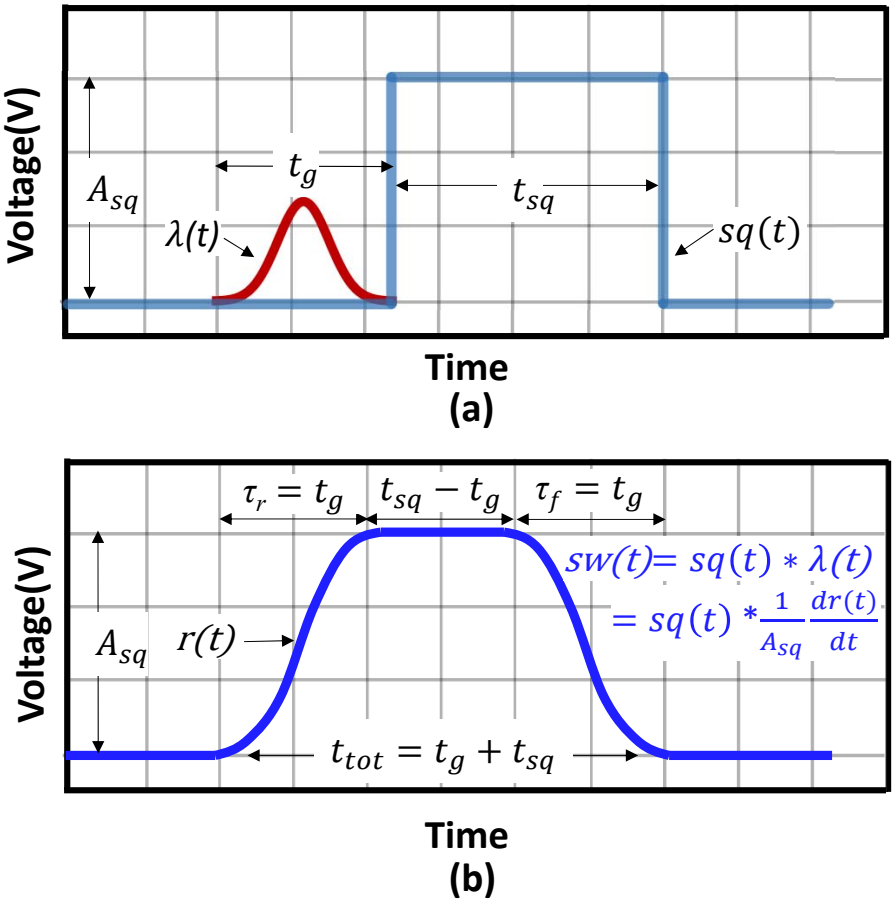


Figure 5.1: (a) Convolution of a square wave and a Gaussian function in order to get a Gaussian switching waveform and (b) the resulting Gaussian switching waveform.

Different from the trapezoidal waveform using the square pulse as $g(t)$, the Gaussian switching waveform uses the normalized Gaussian function $\lambda(t)$ to produce the Gaussian switching. After the convolution of the two waveforms, the total pulse width of the generated Gaussian switching waveform t_{tot} is given by [49]

$$t_{tot} = t_g + t_{sq} = 4\sigma + t_{sq}. \tag{5.2}$$

It can be observed from Fig. 5.1(b) that the fall/rise time of the Gaussian function τ_f/τ_r is equal to t_g. To adjust τ_f/τ_r of the Gaussian switching waveform, standard deviation σ needs to be changed accordingly.

The corresponding Fourier series coefficients of the proposed Gaussian switching waveform is given by

$$SW(F_s n) = A_{sq} t_{sq} F_s \cdot sinc(\pi n F_s t_{sq}) \cdot e^{-\frac{t_g^2 (2\pi n F_s)^2}{16}} \tag{5.3}$$

where F_s is the switching frequency, t_{sq} is pulse width and A_{sq} is the amplitude of the square waveform $sq(t)$ respectively. Fig. 4.2 shows the time-domain waveforms and the corresponding spectra of Gaussian switching and trapezoidal switching. As can be seen, the decay rate of the Gaussian switching increases as the frequency increases towards infinite after the pole located at $\frac{1}{\pi t_{tot}}$ whereas the decay rates of the trapezoidal switching are -20 dB/decade over frequencies between the first and second pole and -40 dB/decade above the second pole. With the Gaussian switching, an exponential decay over frequencies after the only pole in the spectrum is introduced. After the spectrum reaches the null, the noise floor stays at zero for the ideal Gaussian switching. The comparison between the Gaussian switching and the trapezoidal switching is shown in Fig. 5.2.

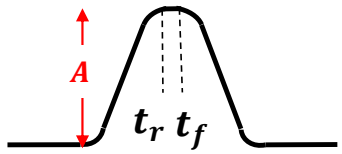
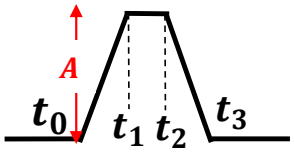
	Gaussian Switching	Trapezoidal Switching
Formula of V_{DS}	$\begin{cases} A \int_{-\infty}^{t_r} \frac{1}{\sigma\sqrt{2\pi}A} exp\left(-\frac{t^2}{2\sigma^2}\right) dt \ (-\infty > t > t_r) \\ A \ (\tau_r > t > \tau_f) \\ A \int_{t_f}^{+\infty} \frac{1}{\sigma\sqrt{2\pi}A} exp\left(-\frac{t^2}{2\sigma^2}\right) dt \ (t_f > t > +\infty) \end{cases}$	$\begin{cases} \left(\frac{A}{t_r}\right) t \ (t_0 > t > t_1) \\ A \ (t_1 > t > t_2) \\ -\left(\frac{A}{t_r}\right) t \ (t_2 > t > t_3) \end{cases}$
Poles	$1/\pi\tau$	$1/\pi\tau \ ; \ 1/\pi\tau_r$
Decay rates	$aproaching \ -\infty$	-20 dB/decade; -40 dB/decade
Transient waveform		

Figure 5.2: Comparison between the Gaussian switching and trapezoidal switching.

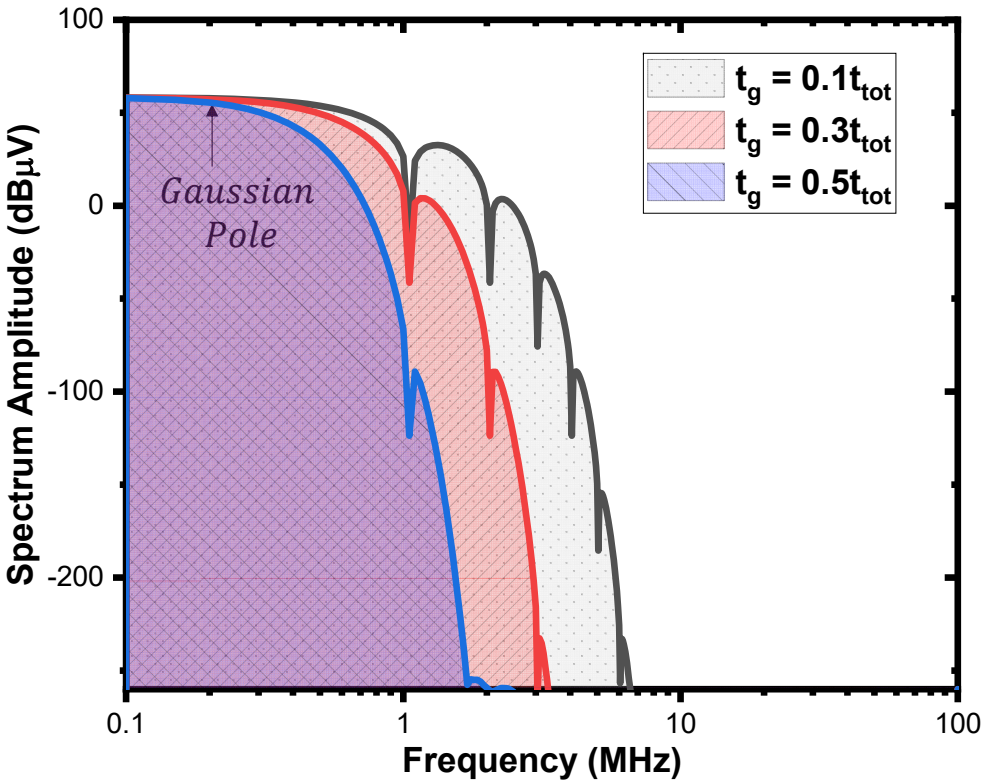


Figure 5.3: Spectra Comparison of Gaussian switching waveforms with same total pulse width t_{tot} but different Gaussian pulse width t_g.

Controlled by the pulse-width modulation (PWM) signal which has a fixed total pulse width t_{tot}, the fall/rise time of the Gaussian function τ_f/τ_r can be increased by applying a larger standard deviation σ, according to (5.2). The simulated spectrum is shown in Fig. 5.3. As can be seen, when t_g (equals τ_f/τ_r) increases from $0.1t_{tot}$ to $0.5t_{tot}$, the pole locations remain the same but the spectral envelopes decay more rapidly over the high-frequency domain. This feature is similar to that of the trapezoidal switching of different fall/rise time but Gaussian switching offers much higher decay rate for EMI reductions above the only pole at $\frac{1}{\pi t_{tot}}$. Based on this feature, by reconfiguring t_g of the Gaussian slope, a tradeoff between the power efficiency and EMI noise can be obtained. The adjustable slew rate of the switching node voltage V_{SW} can significantly reduce the high-frequency EMI noise and allow for simultaneous optimization of the power efficiency by changing the I-V overlapping of the power switches.

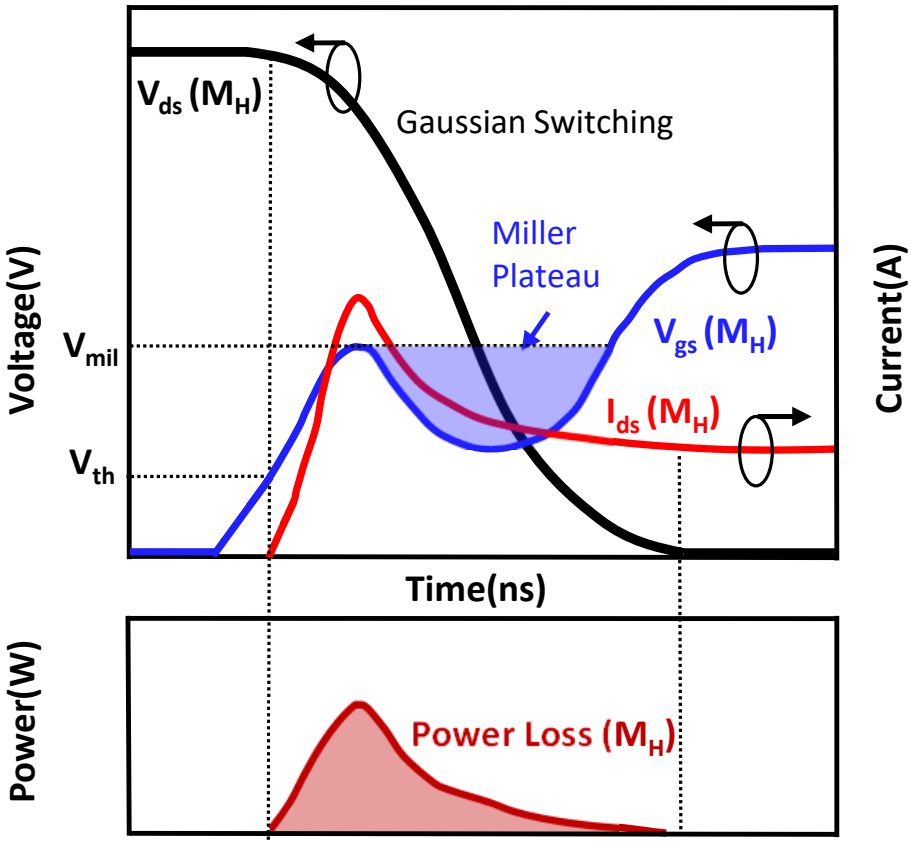


Figure 5.4: Key waveforms and corresponding power loss of the buck converter during turn-on state of the high-side GaN FET M_H.

5.1.2 Gaussian Switching of GaN FET

Fig. 5.4 shows the key waveforms and the corresponding power loss of a GaN-based buck converter during the turn-on state of the high-side switch M_H. After the driving voltage v_{gs} exceeds the threshold voltage V_{th}, M_H is gradually turned on and the drain-source voltage V_{ds} starts to fall from the input voltage V_{IN}. Meanwhile, the switching node voltage V_{SW} starts to rise from near 0 V. At the end of the Miller plateau, V_{SW} reaches to the maximum at V_{IN} and V_{ds} falls to 0 V. During this time interval, the GaN FET operates in the saturation region. To regulate the switching node voltage V_{SW} in the GaN-based buck converter to follow the Gaussian switching trajectory, the switching behavior of GaN devices need to be

studied. The device model of GaN FET in the saturation region is given by [50]

$$v_{ds}(t) = V_{IN} - \int \left\{ \frac{g_m \left[v_{gs}(t) - V_{th} \right] - I_L}{C_{oss}(t)} \right\} dt \tag{5.4}$$

where g_m and V_{th} are the transconductance and the threshold voltage of the GaN FET, I_L is the load current, $v_{gs}(t)$ is the gate-source voltage of the GaN FET, and $C_{oss}(t)$ is the effective output capacitor of the GaN FET respectively. Parameters g_m, I_L and V_{th} are considered as constants. To precisely control v_{gs}, segmented current sources are chosen as the driving circuit to charge/discharge the gate capacitor of the GaN switch to turn on/off the GaN device. Substituting $v_{gs}(t)$ in (5.4) with the capacitance gate-charging equation, the switching node voltage sw(t) is derived as

$$sw(t) = V_{IN} - v_{ds}(t) = \int \left\{ \frac{g_m \left[\frac{I_g(t) \cdot t}{C_{iss}(t)} - V_{th} \right] - I_L}{C_{oss}(t)} \right\} dt \tag{5.5}$$

where $C_{iss}(t)$ is the gate capacitance of the GaN FET, and $I_g(t)$ is the driving current from the gate driver. To simplify the analysis, during the rise time of the Gaussian switching when $0 < t < t_g$, the switching node voltage V_{SW} can be derived from (1) as

$$sw(t) = V_{IN} \int_0^t \frac{1}{V_{IN} \cdot \sigma\sqrt{2\pi}} \cdot e^{-\frac{\tau^2}{2\sigma^2}} d\tau \tag{5.6}$$

where V_{IN} is the input voltage of the buck converter. To regulate V_{SW} to follow the Gaussian switching trajectory, equate (5) and (6) and the analytical solution is given by

$$\frac{g_m \left[\frac{I_g(t) \cdot t}{C_{iss}(t)} - V_{th} \right] - I_L}{C_{oss}(t)} = \frac{1}{\sigma\sqrt{2\pi}} \cdot e^{-\frac{\tau^2}{2\sigma^2}}. \tag{5.7}$$

As can be observed from the left-hand side of (5.7), $v_{gs}(t) = \frac{I_g(t) \cdot t}{C_{iss}(t)}$ behaves like a driving current charging C_{iss} over the rise time of V_{SW}. However, the right-hand side part of (5.7) is the Gaussian function showing a peak value in the middle of the switching time. To regulate the left-hand side of (6) to resemble the Gaussian function, nonlinearities of the C_{iss} and C_{oss} inside the GaN FET are utilized when it is operating in the saturation region. Fig. 5.5 shows

the simulated C_{iss} with respect to v_{gs} when $v_{ds} = 30V$ and C_{oss} with respect to V_{ds} when $v_{gs} = 2.0V$ [51]. As can be observed, C_{iss} is positively correlated to v_{gs} after v_{gs} enters the Miller plateau and C_{oss} is negatively correlated to V_{ds}. During the turn-on procedure, when v_{gs} reaches the threshold voltage V_{th}, C_{oss} starts to increase as V_{ds} decreases. As v_{gs} continues to increase and reaches the Miller plateau voltage V_{mil}, C_{iss} starts to increase rapidly which causes v_{gs} and the left-hand side of (5.7) starts to fall in the middle of the Miller plateau. During the second half of the Miller plateau, as the driving current continuous to charge the saturated C_{iss} and v_{gs} starts to rise again. Meanwhile, V_{ds} decreases rapidly which causes strong increase of C_{oss} which maintains the slow decline of the left-hand side of (5.7). GaN C_{oss} and C_{iss} are one order of magnitude smaller compared to Silicon-based power MOSs with similar on-resistances therefore make it possible to implement Gaussian regulation at a very high speed [50].

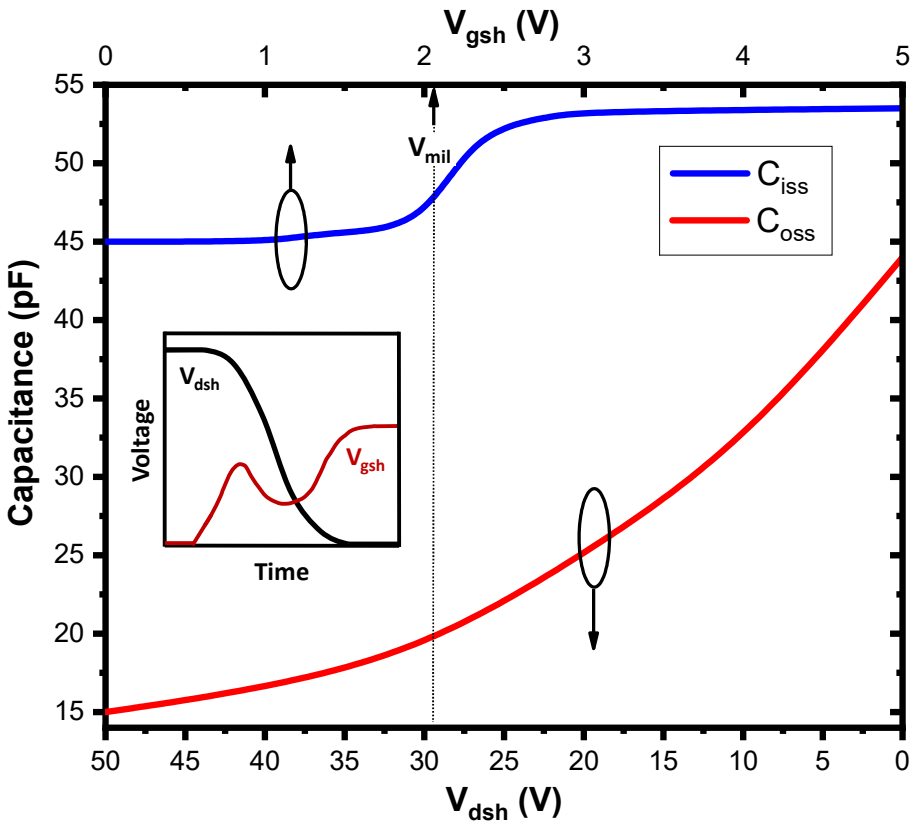


Figure 5.5: Simulated C_{iss} with respect to v_{gs} and C_{oss} with respect to V_{ds} during turn-on state of the upper GaN switch M_H.

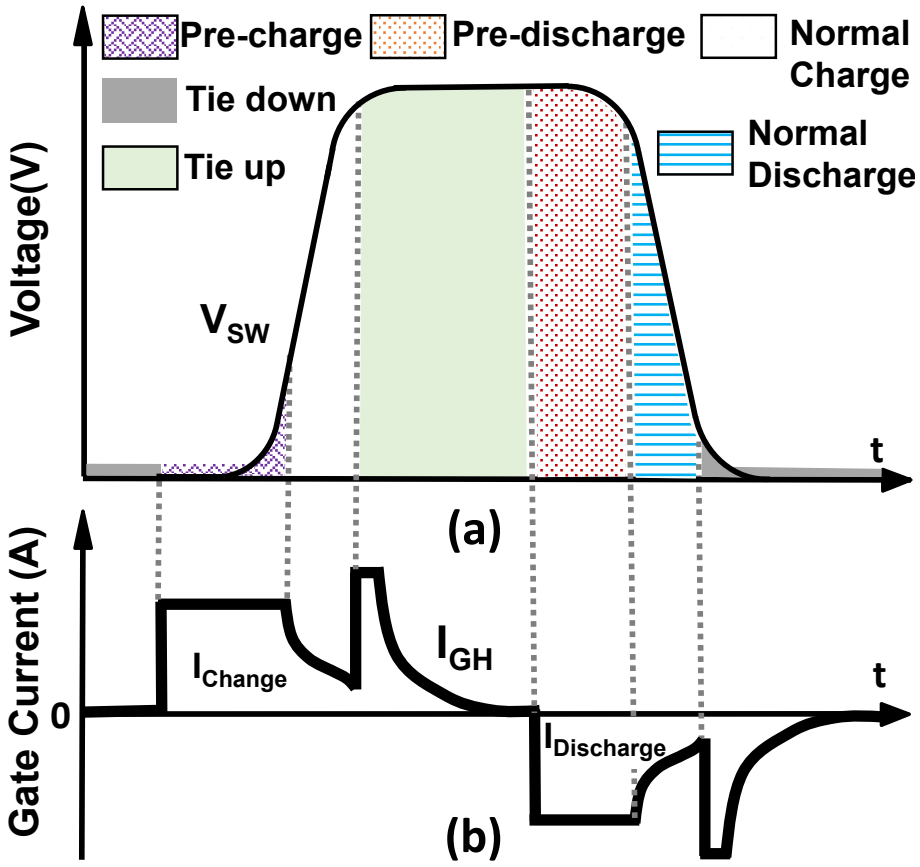


Figure 5.6: The proposed 6-phase Gaussian regulation on the switching node voltage V_{SW} (a) and the corresponding gate current I_{GH} (b).

5.1.3 Feed-forward Slope-Reconfigurable Gaussian Switching Regulation

As mentioned in Section 5.1, the nonlinear capacitors C_{iss} and C_{oss} make it possible to realize Gaussian switching by GaN FET. Conventional Gaussian regulation scheme based on a feedback loop and error amplifier/ADC can only deal with relatively low switching frequency f_{SW} (typically less than 1 MHz). With the increased switching frequency f_{SW} with GaN devices, the requirements on bandwidth and power consumption of the feedback loop would be too stringent for an on-chip feedback loop implementation. To precisely regulate the Gaussian switching, a feed-forward current-mode gate driving scheme is proposed to drive the high-side GaN M_H to generate an accurate Gaussian switching on the switching node. In the proposed scheme, each rising edge of V_{SW} is divided into three phases and

during each phase one current pulse charges the gate of M_H. Similarly, the falling edge of V_{SW} is also divided into three phases during which the gate of M_H is discharged by three current pulses respectively. To optimize the power efficiency, the slew rate of the Gaussian switching can be adjusted by reconfiguring the pulse widths and magnitudes of the driving current.

Fig. 5.6 illustrates the proposed feed-forward gate-driving scheme and its corresponding V_{SW} and gate current to the M_H (I_{GH}). To precisely generate the Gaussian trajectory, each cycle of V_{SW} is divided into six phases: pre-charge/pre-discharge, normal-charge/normal-discharge and tie-up/tie-down, which are controlled by six tunable segmented current sources respectively. Prior to applying the Gaussian gate driver, a calibration mode is applied to the Gaussian gate driver to extract the parameters for the six operational phases. In the calibration mode as shown in Fig. 5.7, the Gaussian reference is realized off-chip by a 6-order passive Gaussian filter driven by a square wave from a signal generator [52]. The parameters of the circuits such as the pulse widths and magnitudes of the driving currents are obtained by fitting the curves of V_{SW} with the Gaussian reference waveforms. The extracted parameters are converted into voltage biases on the chip to generate the required current pulses during the applications. According to Fig. 5.3 with Gaussian regulation scheme, to improve the existing EMI profile, longer Gaussian switching times can be adopted with the penalties of power efficiency. With the reconfigurable Gaussian switching time, optimizations between the power efficiency and EMI standard are realized.

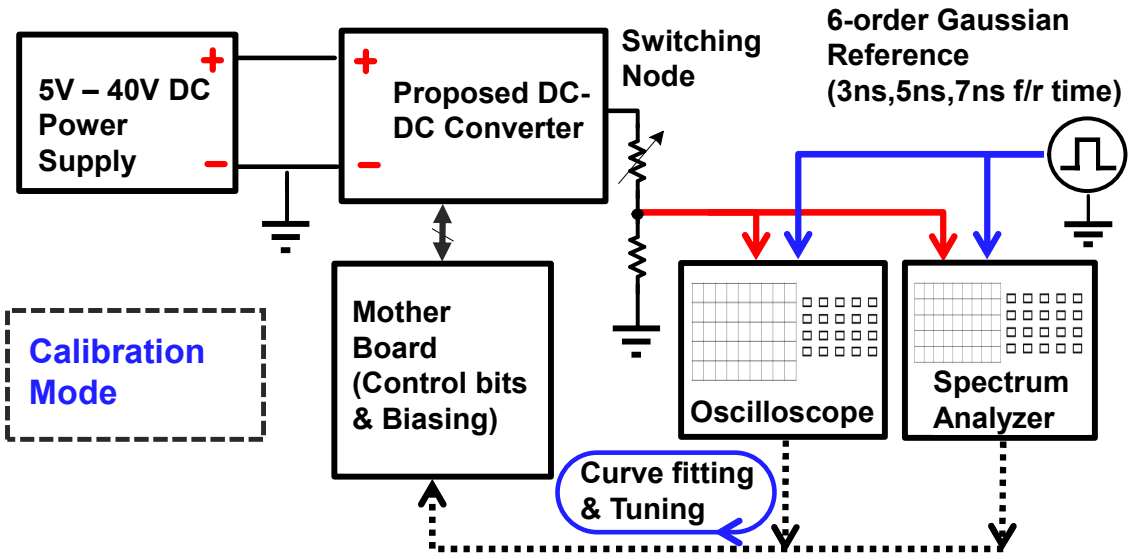


Figure 5.7: Calibration setup to obtain parameters in the six operational phases.

5.1.4 Spread-Spectrum Frequency Dithering with Gaussian Switching Regulation

The proposed SSFD scheme can be simplified as single-tone frequency modulation in a wide band [53]. The generated $sw(t)$ by SSFD can be analyzed as a sine wave f_c at the carrier frequency (equal to the undithered f_{SW}) modulated by a single tone f_m which is denoted as

$$sw(t) = A_c cos\left[2\pi f_c t + \beta sin(2\pi f_m t)\right] \tag{5.8}$$

where A_c is the magnitude of the carrier, β is the modulation index which is defined as the variation of the modulation frequency ($\triangle f_M$) divided by the modulation frequency (f_m) as [54]

$$\beta = \frac{\triangle f_m}{f_m}. \tag{5.9}$$

Using Bessel functions of nth order (J_n), (8) can be regrouped as

$$sw(t) = A_c \sum_{n=0}^{\infty} J_n(\beta) cos\left[2\pi(f_c + n f_m)t\right] \tag{5.10}$$

The waveform in (5.9) contains both fundamental and harmonic spurs. Around the fundamental frequency, the amplitude attenuation after using SSFD is expressed as $2\pi\beta$ which is proportional to the modulation index β. A higher β value is required to lower the energy level in the low-frequency band. However, since the total amount of spectrum energy is unchanged if only SSFD is applied, more energy is reduced in the low-frequency domain while some of the EMI noise is moved towards the high-frequency domain. This is where Gaussian switching regulation can be also applied to counteract the increased high-frequency harmonic energy by attenuating the high-order harmonics. Similar to the analysis in Section 5.1, the switching node signal with Gaussian switching regulation along with SSFD scheme is given by

$$sw(t) = A_c \sum_{n=0}^{\infty} J_n(\beta) cos\left[2\pi(f_c + nf_m)t\right] * \left(\frac{e^{-\frac{t^2}{2\sigma^2}}}{\sigma_t\sqrt{2\pi}}\right). \tag{5.11}$$

The combined EMI-reduction of the two schemes can be evaluated as (5.12) by performing Fourier transform of (5.11)

$$s(f) = \frac{A_c}{2} e^{-\frac{t_g^2(2\pi f)^2}{16}} \sum_{n=0}^{\infty} J_n(\beta)\left[\delta(f - f_c - nf_m) + \delta(f + f_c + nf_m)\right] \tag{5.12}$$

where t_g is the pulse width of the Gaussian function. As can be seen from (5.12) by increasing the modulation index β, the spectrum of the spurs can be compressed more evenly. Above the pole in the high-frequency band, the exponential decay introduced from the Gaussian switching regulation is crucial to attenuate the high-order harmonic noises.

Spectrum analysis on the conducted EMI noise with different EMI reduction techniques is shown in Fig. 5.8. After applying the 5% SSFD to the conventional trapezoidal switching at 10 MHz with 7 ns fall/rise time, the noise level is deduced by 24 dB at f_{SW} and more than 10 dB towards the high-frequency domain. With Gaussian regulation only with 7 ns fall/rise time, the EMI noise is exponentially attenuated towards high frequencies but remains unchanged below the Gaussian pole which agrees well with the theocratical analysis. With both techniques applied, the proposed GaN driver can achieve excellent EMI reduction over the entire frequency band. In the low-frequency band, the noise reduction is as good as the results of using SSFD only. In the middle-frequency range, the noise reduction is at least 15 dB better than that of using Gaussian regulation only. In frequencies above 100 MHz,

the noise envelope is slightly higher than that from using the Gaussian regulation alone but still tens of dBs lower than the results from using SSFD only. The EMI degradations above 100 MHz before and after adopting the SSFD technique are caused by the energy spread from low-frequency domain to the high-frequency domain due to SSFD. The Gaussian and SSFD schemes are compatible and complementary with each other in term of reducing EMI.

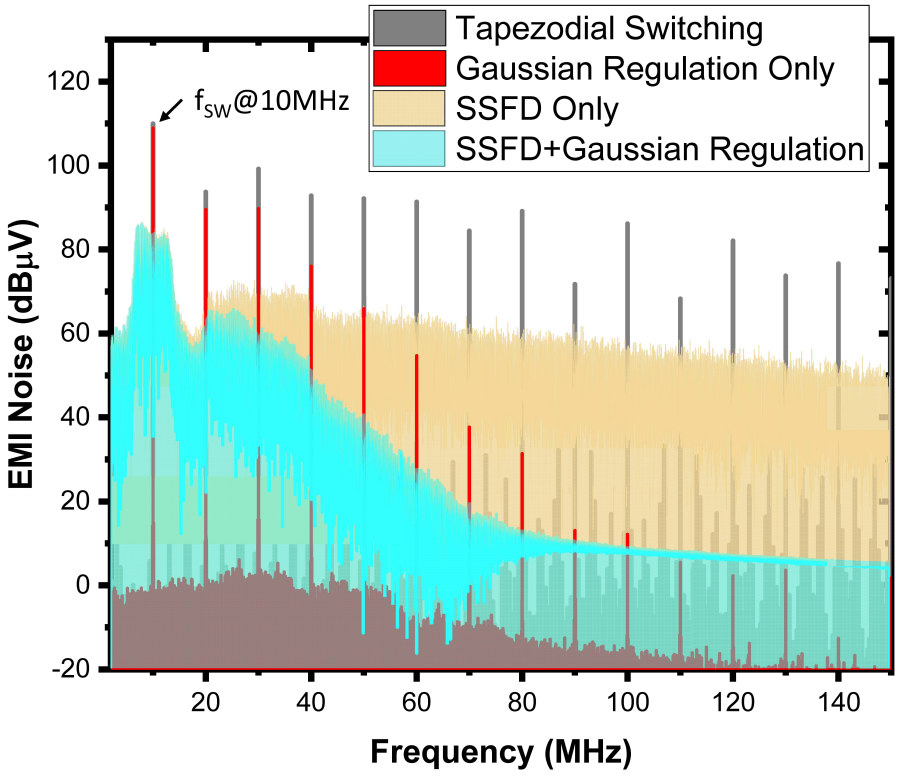


Figure 5.8: Simulated EMI noises without/with Gaussian Regulation and SSFD schemes.

5.2 Circuit Design and Implementation

The system architecture of the proposed GaN-based buck converter operating at 10 MHz f_{SW} with reconfigurable EMI reduction is illustrated in Fig. 5.9. Instead of using conventional trapezoidal switching, the proposed architecture employs a 6-phase current-mode gate driver to produce a near Gaussian switching voltage V_{SW} at the switching node. To opti-

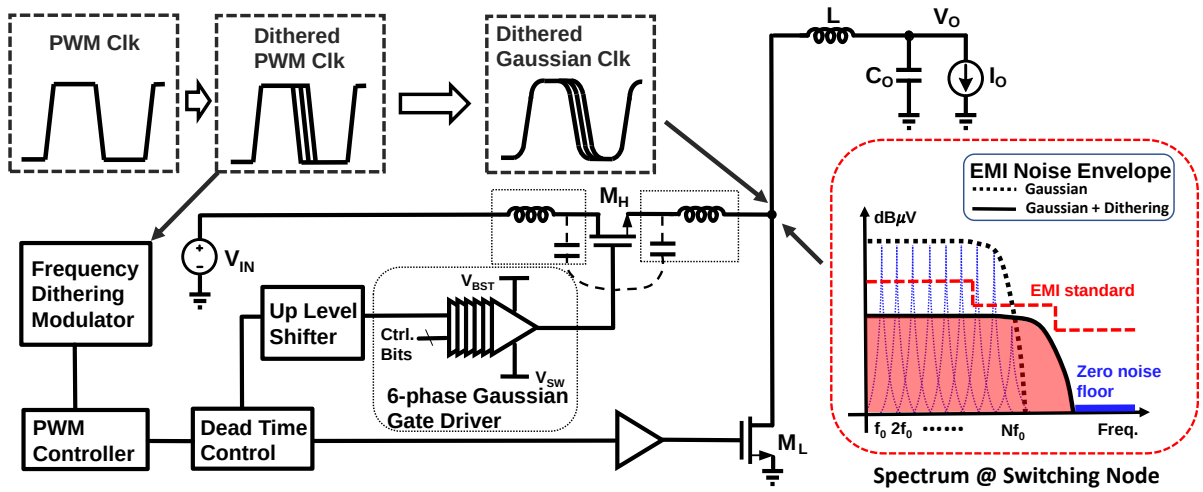


Figure 5.9: Proposed DC-DC converter based on Gaussian regulation and SSFD schemes.

mize the power efficiency, a reconfigurable fall/rise time (τ_f/τ_r) of the Gaussian switching is realized to tradeoff between power efficiency and EMI noise. The proposed driving scheme is capable of generating a precise Gaussian V_{SW} to significantly reduce EMI at frequencies above the pole $\frac{1}{\pi t_{tot}}$, which is unachievable by any trapezoidal V_{SW} schemes. In addition, a SSFD scheme is used to dither the (PWM) signal which effectively reduces the EMI in the low-frequency domain. These two methods combined can achieve effective EMI reduction across wide frequency spectrum while maintaining good power efficiency.

5.2.1 Gaussian Regulation Circuit Design

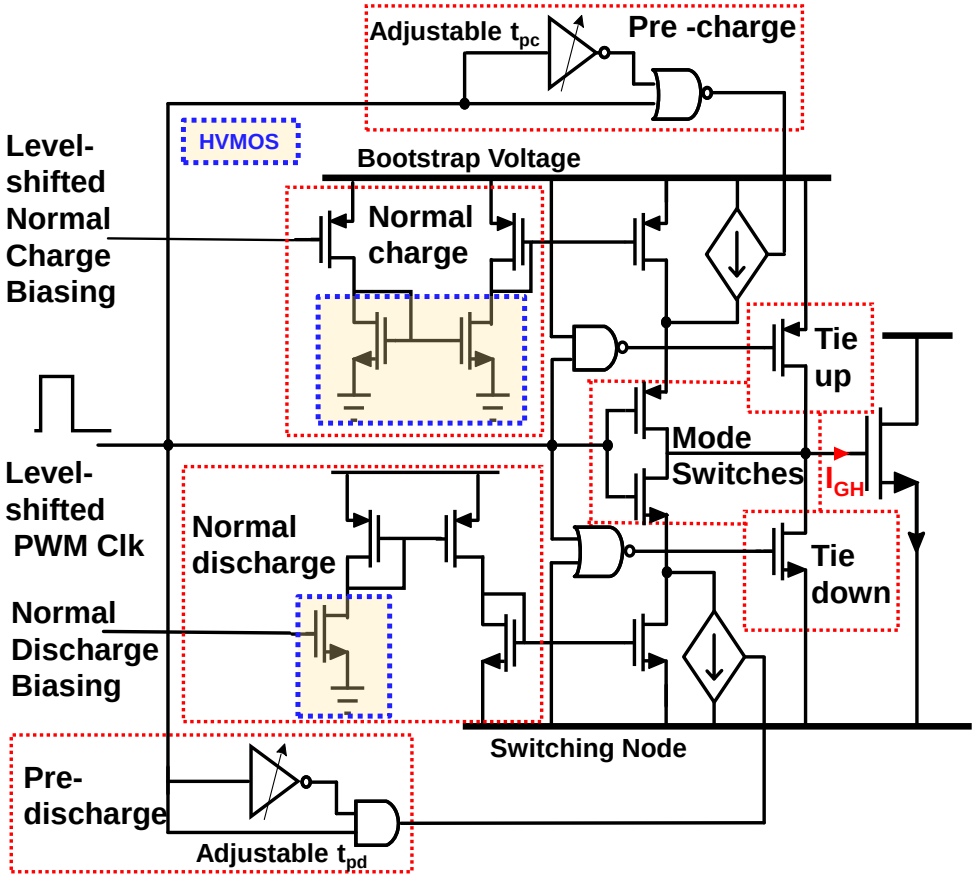


Figure 5.10: Implementation of 6-phase current-mode gate driver to turn on/off M_H.

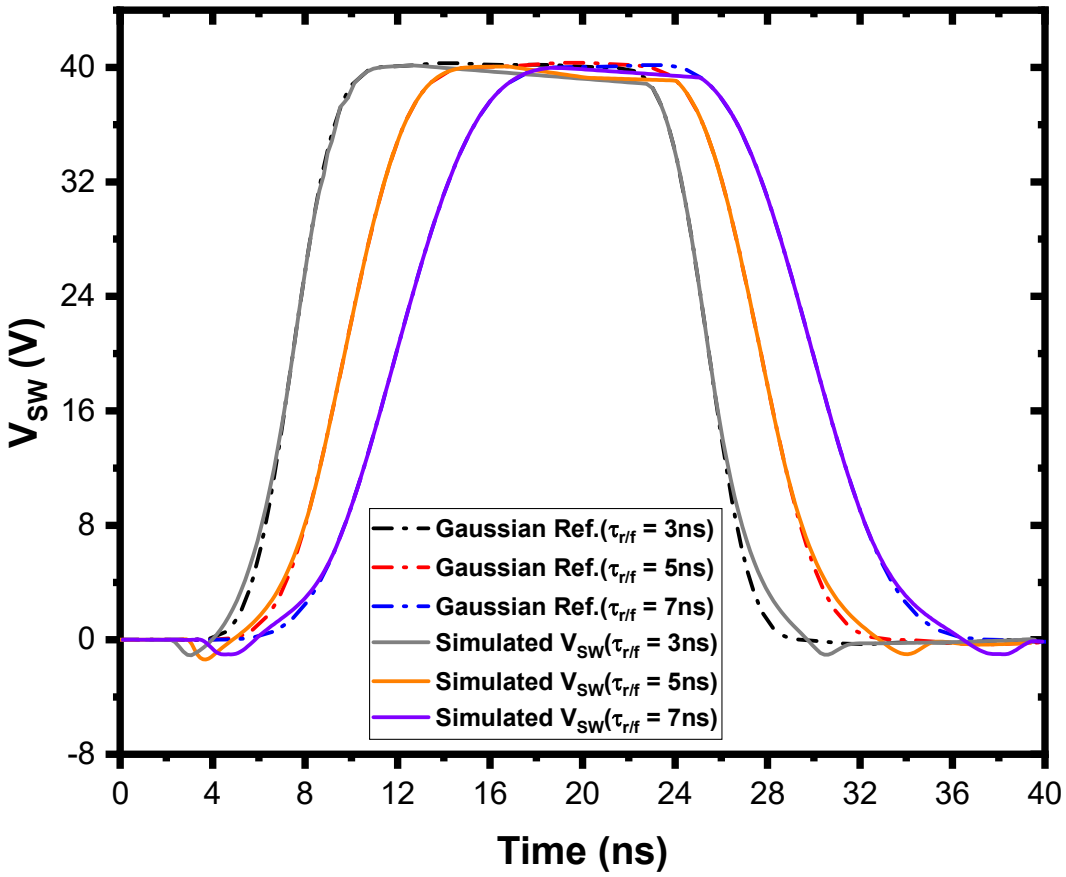


Figure 5.11: Simulated V_{SW} of the proposed Gaussian gate driver with 3 ns, 5 ns and 7 ns fall/rise time in comparison with ideal Gaussian references.

The on-chip Gaussian regulation circuit is illustrated in Fig. 5.10. Current-mode driving using segmented current sources is adopted to charge/discharge the high-side GaN device M_H. The biasing voltages for the pre-charge/pre-discharge and normal charge/normal-discharge are individually tunable by using an high-voltage (HV) NMOS as down-level shifters to sustain a boot strap voltage (V_{BST}). To optimize the power efficiency, the fall/rise time τ_f/τ_r of the Gaussian V_{SW} are designed to be reconfigurable by individually adjusting the pre-charging/discharging time (t_{pc}, t_{pd}) and the biasing currents for the segmented current source. There are three HV NMOS devices employed in the gate driver as outlined in Fig. 5.10. As illustrated in Fig. 5.6, the Gaussian regulation scheme is divided into 6 phases. Triggered by the rising edge of the level-shifted PWM signal, the pre-charge and

normal-charge current sources charge the gate of M_H together which provides a high I_{GH} to quickly drive the gate voltage of M_H to reach the threshold voltage at 1.4 V before V_{SW} rises up. After V_{SW} approaches the mid-point of the rising edge, the pre-charge current source is turned off and only the normal charge for smaller driving strength is kept on. After V_{SW} passes the turning point towards the input voltage (V_{IN}), a tie-up circuit is triggered to pull up V_{SW} to V_{IN} instantly meanwhile the normal charge is switched off to reduce the power consumption. Similarly, the pre-discharge and normal discharge are triggered one-by-one followed by the falling edge of PWM signal.

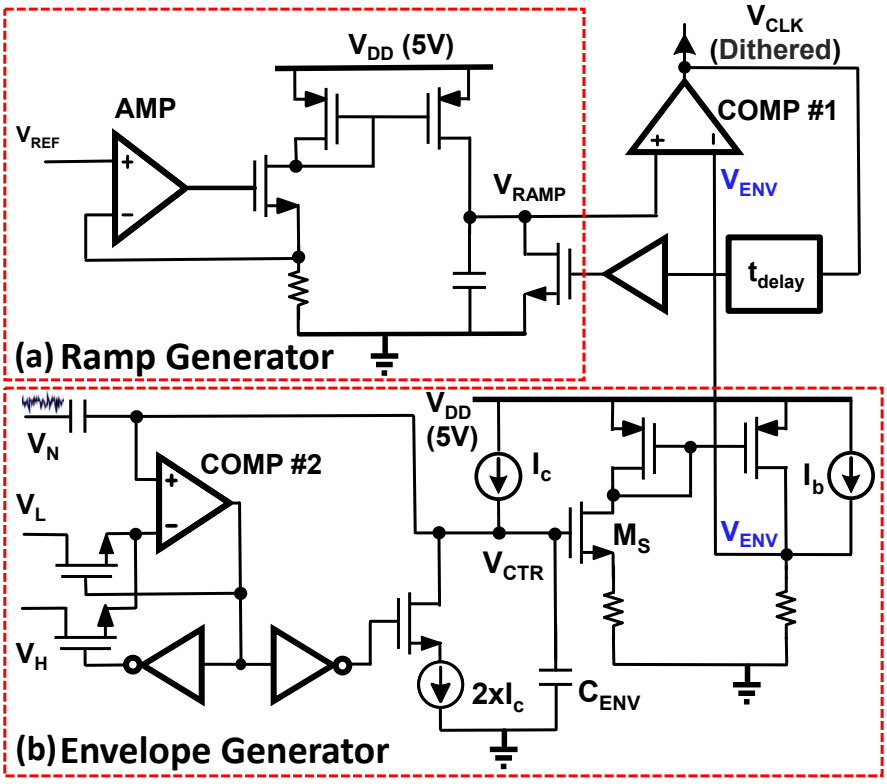


Figure 5.12: Implementation of the SSFD circuit in the converter.

The simulated V_{SW} of the proposed Gaussian gate driver with reconfigurable switching times is shown in Fig. 5.11. The generated V_{SW} waveforms agree well to the Gaussian

references with 3 ns, 5 ns and 7 ns fall/rise time. Compared to the ideal Gaussian references, the distortions exist at the beginning of the rising edges and the end of the falling edges which are introduced from negative V_{SW} during the dead time of the buck converter. Declining slopes exist over the high states of V_{SW}, due to the conduction losses of the M_H that increase with the rising inductor current during each switch-on cycle.

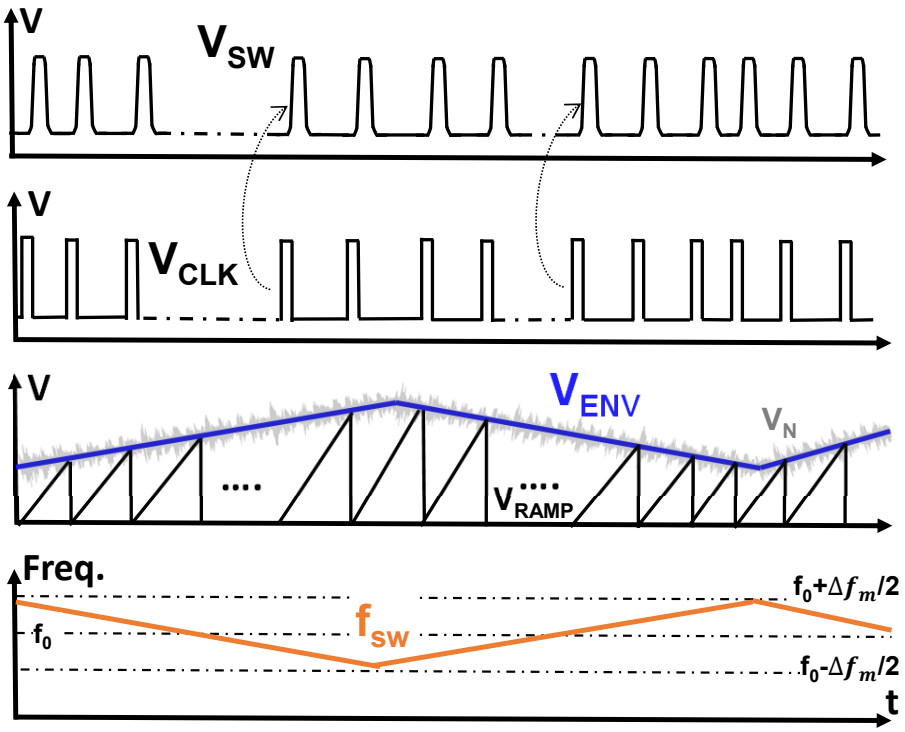


Figure 5.13: SSFD with key operation waveforms of the converter.

5.2.2 Spread-Spectrum Frequency Dithering Circuit Design

The circuit to implement the SSFD is shown in Fig. 5.12. It mainly consists of a ramp generator, an envelope generator and a comparator. The ramp generator and the comparator operate as a pulse width modulation (PWM) signal generator. Fig. 5.12(a) depicts the ramp generator where a relaxation oscillator is adopted to produce a saw-tooth ramp waveform

signal V_{RAMP}. V_{RAMP} is then fed as one of the inputs to the comparator $COMP\#1$. A periodic reference (V_{ENV}) is the other input of the $COMP\#1$ in the PWM signal generator. High-frequency random noise (V_N) provided by the external signal generator is added upon the envelope signal V_{ENV} which modulates the generated ramp signal V_{RAMP} in the comparator. The noisy V_{ENV} dithers the frequency of the PWM signal. The envelope generator is realized by another relaxation oscillator to generate V_{ENV} with tunable peak, valley and average voltage levels. As shown in Fig. 5.12(b), a constant current (I_C) charges capacitor C_{ENV}. The peak and valley voltages of the charged ramp voltage V_{CTR} are determined by the reference levels V_H and V_L respectively. A source follower made of transistor M_S passes V_{CTR} to an adjustable level shifter to produce a triangle wave as V_{ENV}. As illustrated in Fig. 5.13, V_{RAMP} is compared to V_{ENV} in $COMP\#1$ and once it hits V_{ENV} a rising edge of V_{CLK} is generated. After a certain time t_{delay} which determines the high-state time of V_{CLK}, the V_{CLK} rising edge is fed back to short V_{RAMP} to ground to generate the falling edge of V_{CLK}. As V_{ENV} changes periodically, the off-time of V_{CLK} varies in a similar way. Therefore V_{CLK} is dithered with a sideband of Δf_m. After being translated from V_{CLK} by the PWM controller, the switching frequency f_{SW} and its harmonics peak energy levels are compressed effectively.

5.2.3 Gaussian Gate Driver for Three-Level Buck Converter with Zero-Voltage-Switching

For high input voltage with V_{IN} more than 40V, the conventional two-level buck has voltage drops of V_{IN} across each of the two power switches which result low power efficiency. To improve the power efficiency, the architecture of the proposed 48V three-level buck converter with Gaussian switching regulation and zero-voltage-switching is shown in Fig. 5.14. Compared to the conventional two-level buck converter which has two power switches, the three-level buck converter introduce two more power switches and a flying capacitor C_f [55]. Under balanced condition, the voltage across C_f V_{cf} is half of V_{IN}. Therefor, the voltage drop across each of the power switches is halved under the same V_{IN}. Fig. 5.15 shows the power losses inside the power switches from the two-level and three-level buck converters. One can observe that the three-level buck can ideally reduce the power losses to $\frac{1}{4}$ by halving the voltage across power switches. The operation principle of the three-level buck in comparison

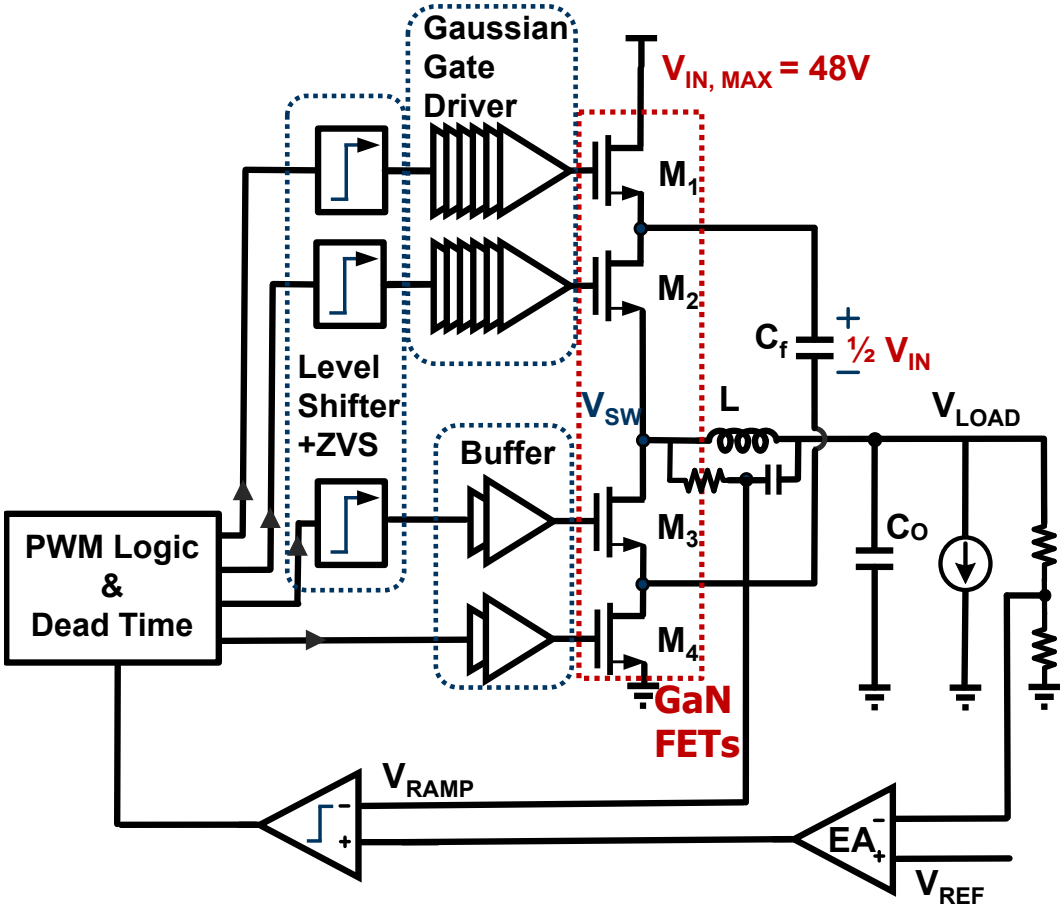


Figure 5.14: The architecture of GaN-based three-level buck converter with Gaussian switching regulation and zero-voltage-switching.

with the two-level buck is shown in Fig. 5.16. For conventional two-level buck, there are two states: on-state and off-state. During the on-state, V_{IN} powers the output stage via the high-side switch. During off-state, output stage is connected to the ground via body diode of the low-side switch. Similar to the two-level buck converter, two on-states (phase 1 and phase 3) and two off-states (phase 2 and phase 4) exist during each cycle of the three-level buck converter as shown in Fig. 5.16. During phase 1, V_{IN} charges C_f and at the same time powers the output stage. During phase 2, the output stage is shorted to ground which is similar to the off-state of the two-level buck. During phase 3, the output stage is powered by V_{cf} only and phase 4 is exactly same to phase 2.

To further improve the power efficiency, zero-voltage-switching (ZVS) detectors are in-

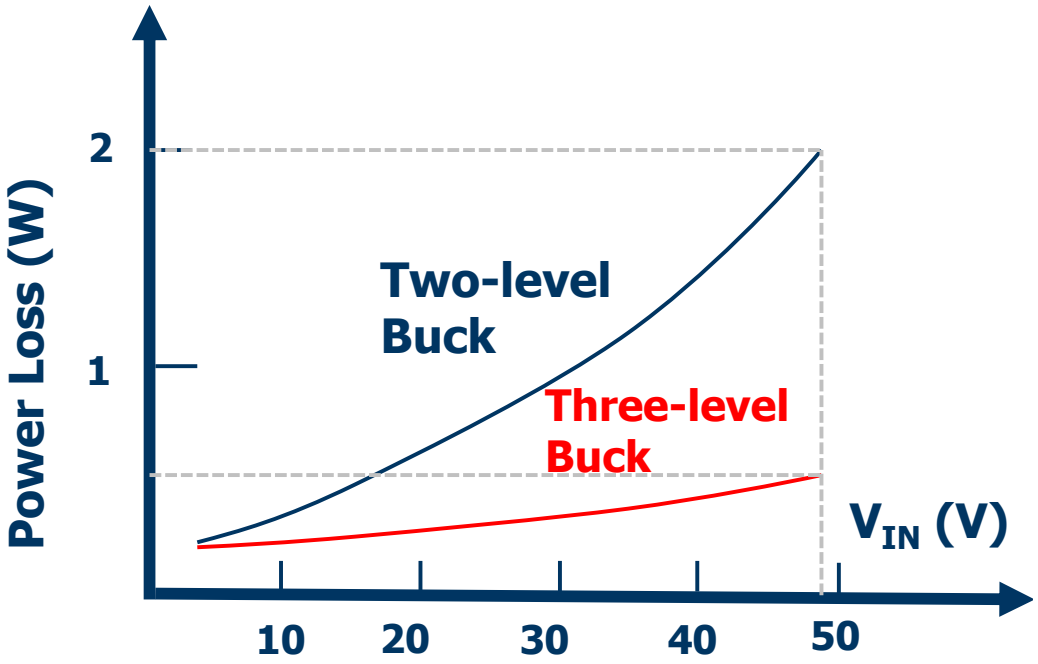


Figure 5.15: Power losses inside the power switches from two-level and three-level buck converters.

troduced to sense the right moments to switch on the power switches. Fig. 5.17 illustrates the key waveforms of a power switch from a buck converter during the switch-on. For an ideal ZVS operation, the gate voltage should be exerted right after the V_{DS} falls to 0 V. If V_{GS} starts to rise before V_{DS} falling to 0 V, there will be a conduction loss inside the power switch. On the other hand, if the dead time is overlength, power loss inside the parasitic body diode will occur. To achieve a precise ZVS detection, a ZVS detector based on HV Schottky diode is proposed as shown in Fig. 5.18. The V_C generated by the biasing circuits is around 1.2V. When V_D starts to fall and reaches V_C, the Schottky diode is turned on which will trigger the falling edge detector and generate the PWM clock to the Gaussian gate driver. The ideal ZVS can be achieved by properly tuning the V_C. Compared to conventional ZVS detector based on body diode inside the power MOSFET [56], the HV Schottky diode has lower conduction voltage drop and faster flipping speed which achieves a more accurate ZVS detection.

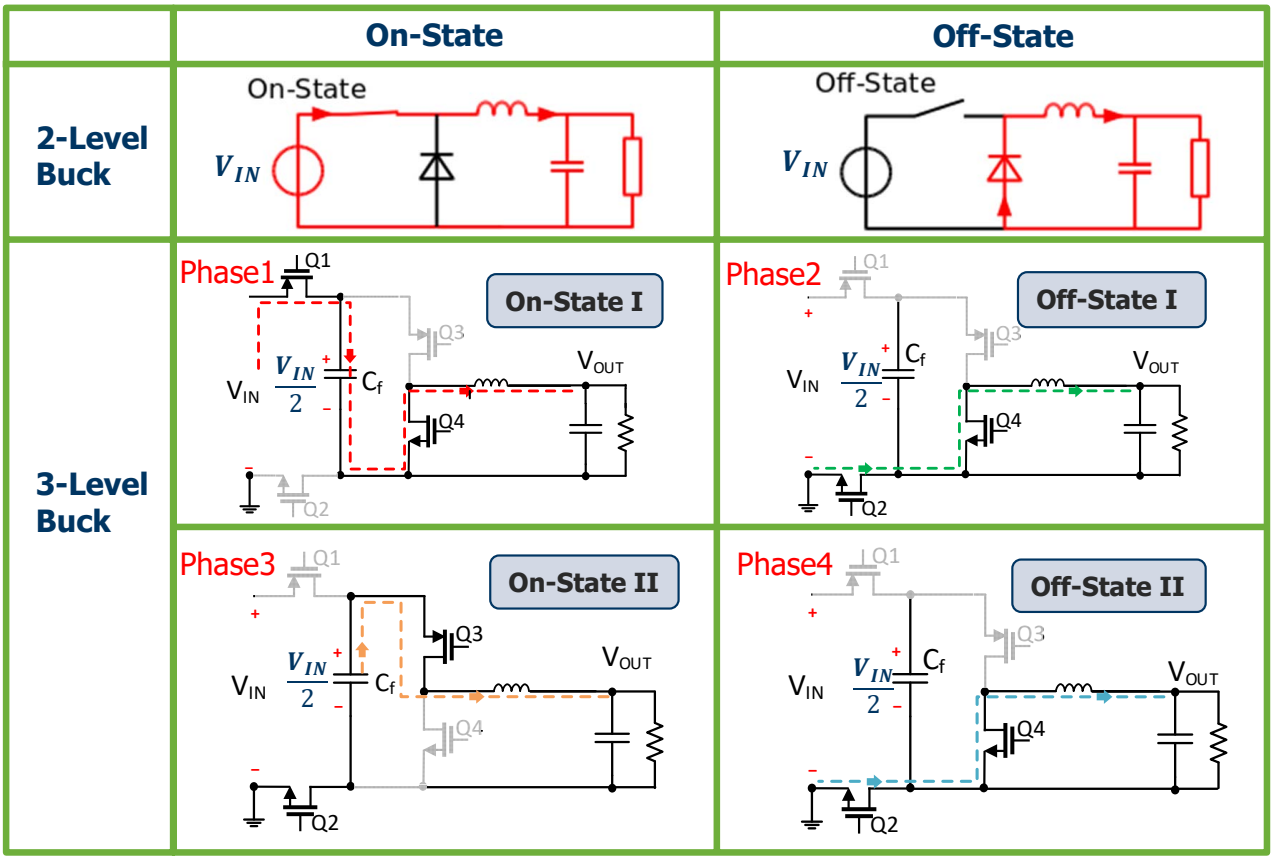


Figure 5.16: Operational modes of two-level buck and three-level buck.

5.3 Experimental Results

The proposed converter is fabricated in 0.18 μm HV BCD process and it occupies a 2.8 mm^2 chip area as shown in Fig. 5.19(a). Two enhancement-mode GaN FET switches are employed as the off-chip power switches. At f_{SW} =10 MHz, a maximum load current (I_O) is achieved at 1.3 A over a V_{IN} ranging from 4 V to 40 V. As mentioned in Section 5.1, calibration to extract the parameters for the Gaussian regulation is done at the beginning of the measurements. To capture the conducted EMI noise from the presented DC-DC converter, a 5 μH line impedance stabilization network (LISN) is connected between the power supply and the buck converter. Then the conducted EMI noise is sent to the spectrum analyzer as shown in Fig. 5.19(b). A 1 μF output capacitor and a 470 nH inductor are used in the power stage.

Table 5.1: Performance Comparison.

	VLSIC 2017 [43]	TVLSI 2013 [38]	JSSC 2018 [42]	JSSC 2019 [39]	This Work
Power Switches	GaN HEMT	MOSFET	GaN HEMT	GaN HEMT	GaN HEMT
Maximum V_{IN}	40 V	5.5 V	40 V	40 V	40 V
Central f_{SW}	10 MHz	3-6.5 MHz	10 MHz	8.3 MHz	10 MHz
EMI Reduction Technique	Trapezoidal Regulation	Frequency Hopping	SSFD+ Trapezodal Regulation	Randomized SSFD (RSSM)	SSFD+ Gaussian Regulation
Vsw Slew Rate	8.5-20 ns	Fixed	1.2-4.4 ns	Fixed	3-7 ns
Maximum Efficiency	81.4%	85%	85.5%	86.8%	85.2%
Gate Driving Control	Current Mode	Voltage Mode	Current Mode	Current Mode	Current Mode
Peak EMI noise Reduction	19 dB<30 MHz 9 dB>30 MHz	28 dB@3 MHz	40.5 dB@10 MHz 22.5 dB@90 MHz	31 dB@8.3 MHz 35 dB@24.5 MHz	36.9 dB@10 MHz 49.1 dB@100 MHz
IC Process	0.35 μm HV BCD CMOS	0.35 μm Standard CMOS	0.35 μm HV BCD CMOS	0.18 μm HV BCD CMOS	0.18 μm HV BCD CMOS

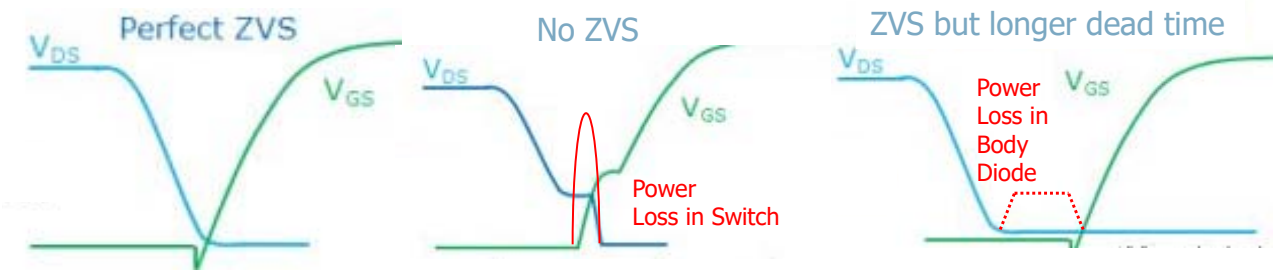


Figure 5.17: V_{GS} and V_{DS} of a power switch during switch-on process.

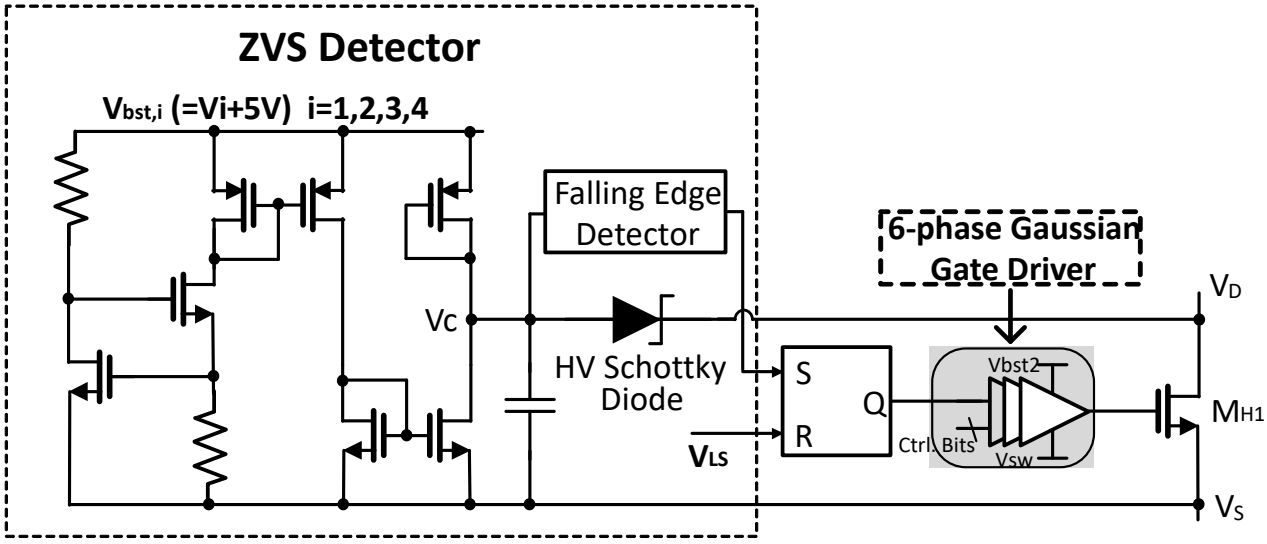


Figure 5.18: Implementation of ZVS detector based on on-chip HV Schottky diode.

The measured V_{gs} of M_H (V_{gsh}) with Gaussian regulation at τ_f=3 ns, 5 ns and 7 ns is presented in Fig. 5.20. By changing the parameters for the 6-phase Gaussian regulation scheme, the shape of V_{gsh} is regulated to produce the required Gaussian V_{SW} with corresponding τ_f/τ_r.

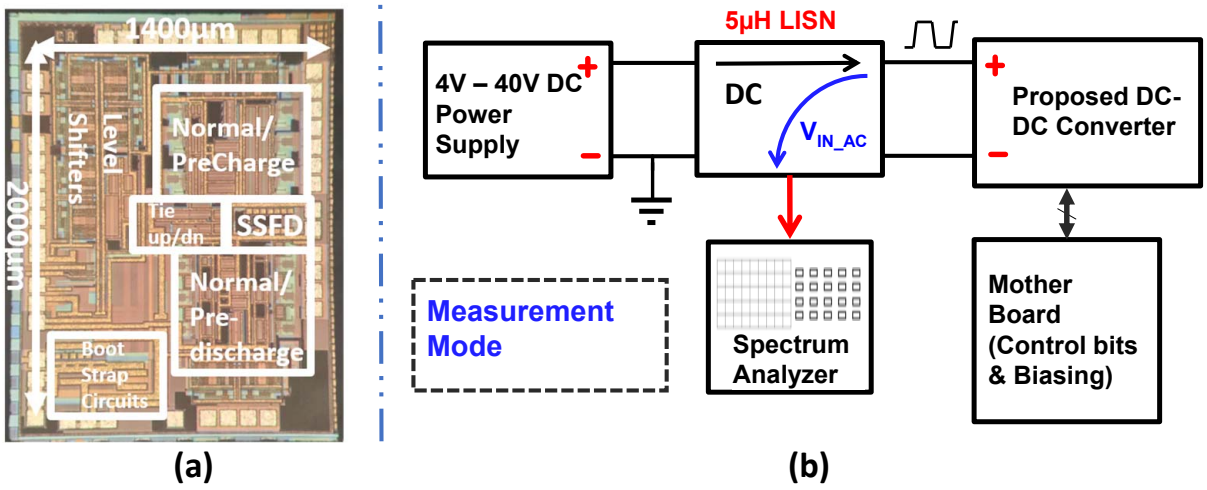


Figure 5.19: (a) Chip micrograph and (b) Conducted EMI-noise test setup.

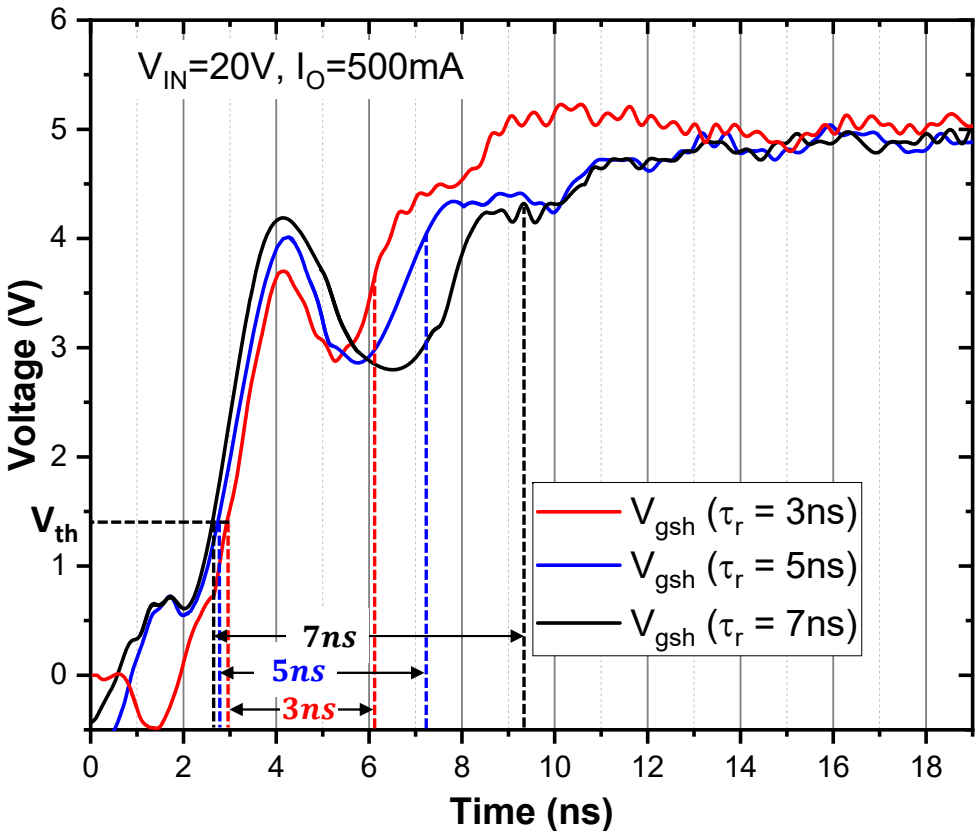


Figure 5.20: Measured V_{gs} of M_H (V_{gsh}) with proposed Gaussian regulation at different τ_r.

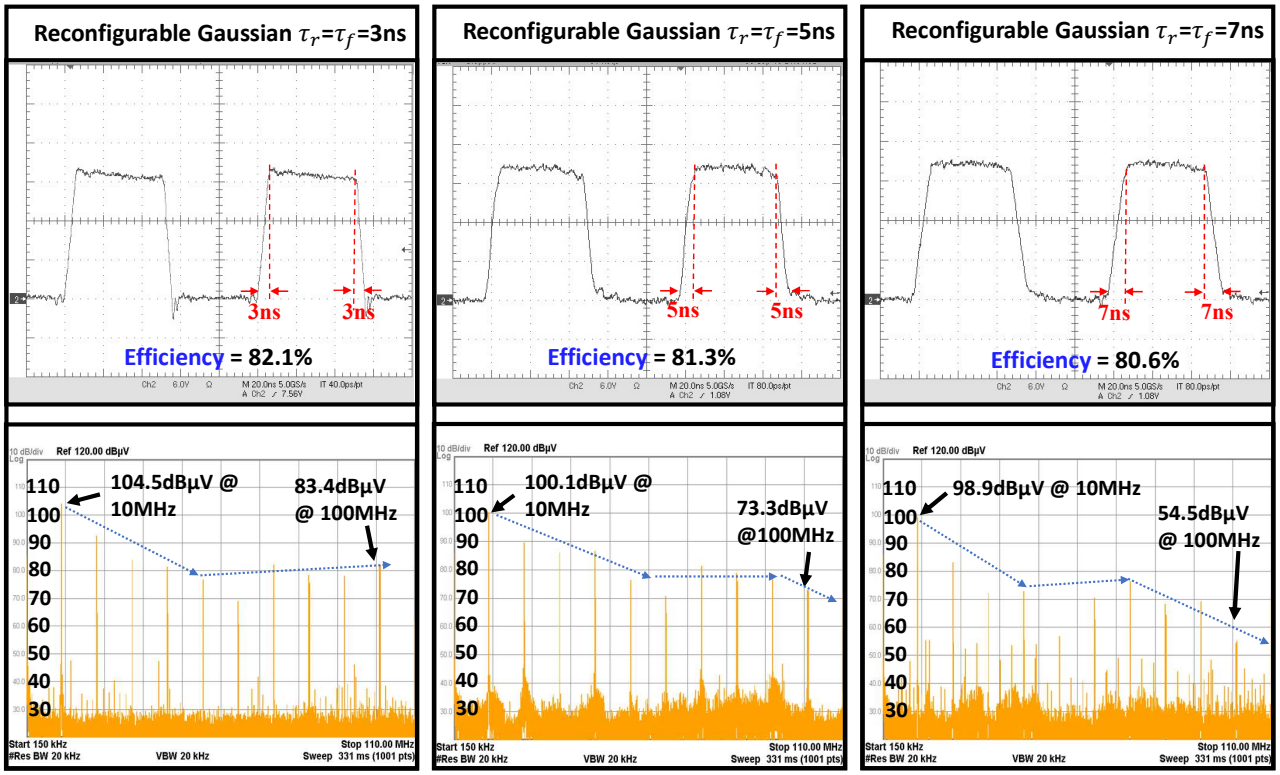


Figure 5.21: Measured waveform and spectrum of V_{SW} with reconfigurable Gaussian regulation scheme.

Fig. 5.21 shows the measured Gaussian V_{SW} and EMI noise spectrum up to 110 MHz when V_{IN}=20 V, τ_{sq}=50 ns with reconfigurable fall and rise time (τ_f/τ_r =3 ns, 5 ns, and 7 ns respectively). From short τ_f/τ_r to long τ_f/τ_r, the spectrum decay rate above the pole increases significantly, which reduces the peak EMI noise at frequencies ≥100 MHz from 83.4 dBμV to 54.5 dBμV with power efficiencies from 82.1% to 80.6%.

Fig. 5.22 shows the comparison of the measured V_{SW} waveform and EMI spectrum in three cases: (a) using conventional trapezoidal switching, (b) using Gaussian (τ_f/τ_r=7 ns) switching, and (c) using Gaussian combined with SSFD scheme with a 5% modulation range. With the Gaussian regulation only, the EMI decay happens above the pole at $\frac{1}{\pi t_{tot}}$ (which is lower than f_{SW}). Compared to the conventional trapezoidal switching, the measured EMI noise at f_{SW} is reduced by 14.3 dB from 113.2 dBμV to 98.9 dBμV; at 100 MHz it is reduced by 49.1 dB from -103.6 dBμV to 54.5 dBμV. When using both Gaussian switching and SSFD schemes, the EMI noise is effectively compressed throughout the entire band. The peak EMI

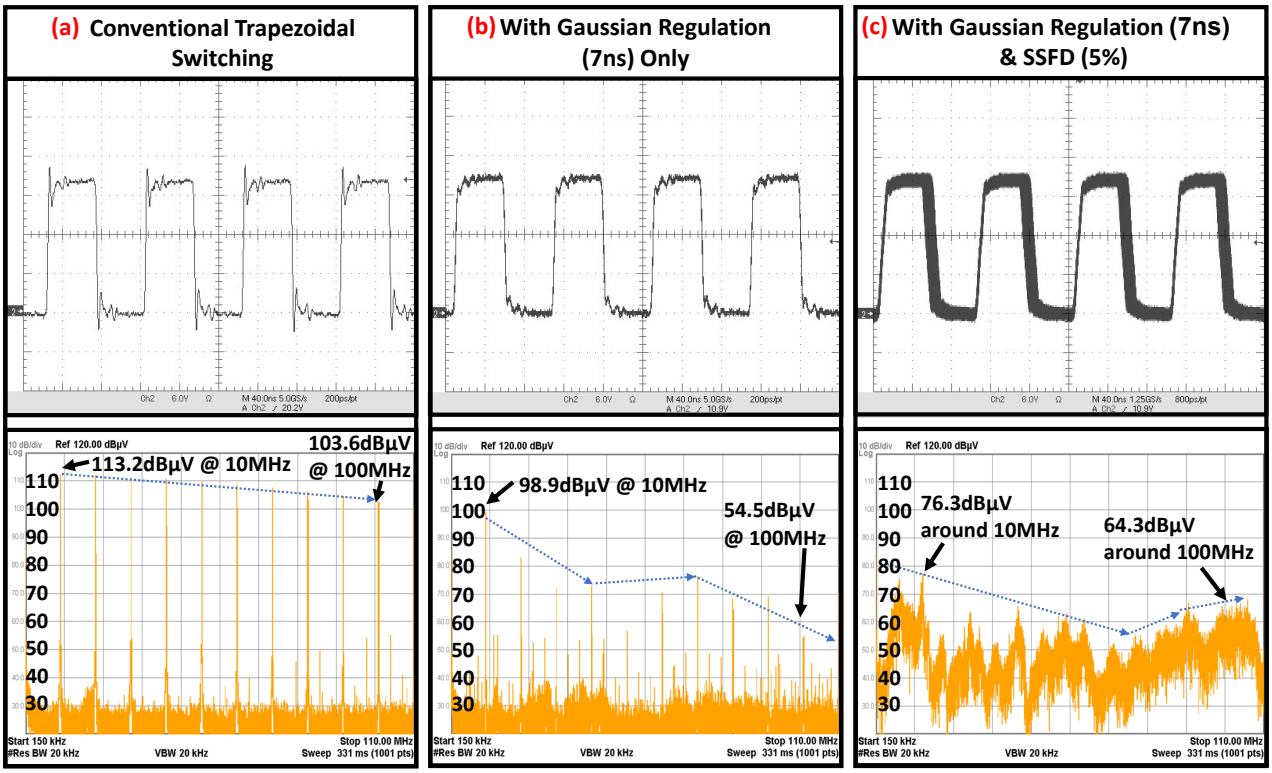


Figure 5.22: Measured waveform and spectrum of V_{SW} with Gaussian regulation and SSFD schemes.

noise reduction is 36.9 dB at f_{SW} (10 MHz) and 39.3 dB at 100 MHz. Due to the energy spread from low-frequency band, there exists a 9.8 dB degradation at 100 MHz before and after adopting the SSFD technique which agree well to the simulation results in Section 5.1.

To further demonstrate the effectiveness of Gaussian switching in terms of EMI reduction, the peak EMI noise is measured over a wider frequency range from 0.2 MHz to 500 MHz, as shown in Fig. 5.23. As can be seen, when using Gaussian regulation (b), the Gaussian spectrum envelope is observed, which reaches a dip at around 100 MHz. Due to the imperfection of Gaussian switching in the actual on-chip implementation, four noise lobes below 78 dBμV are observed as the frequency increases. Combined with the SSFD scheme (c), the peak EMI reduction at mid-frequency range from 100 MHz to 200 MHz is more than 10 dB. From 250 MHz to 400 MHz the measured EMI noise level is below 44.8 dBμV with a peak EMI reduction of 22 dB. Above 400 MHz, the measured peak EMI noise level is reduced by 16 dB at 40.2 dBμV.

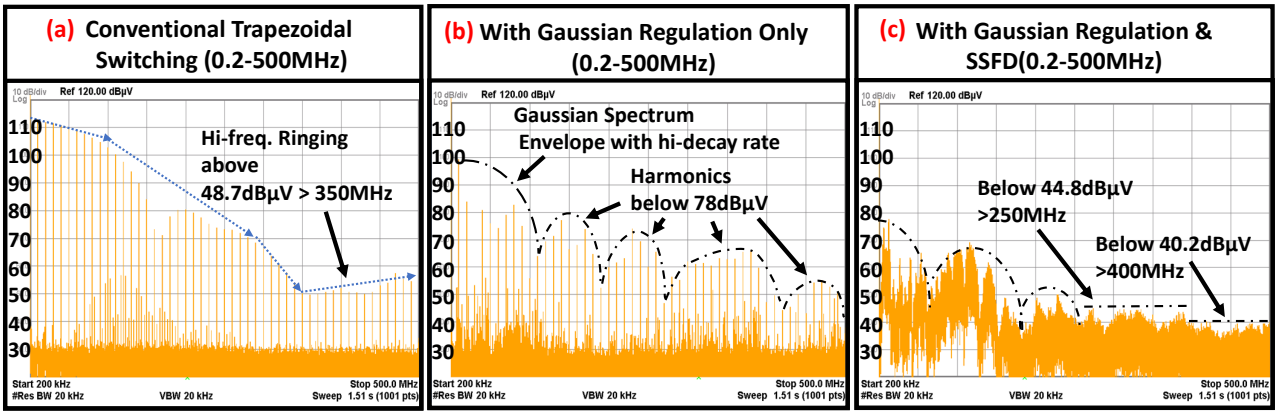


Figure 5.23: Measured conducted EMI noise from 0.2-500 MHz.

Fig. 5.24 shows the measured power efficiency. The peak efficiency is 85.2% for a 12 V-to-5 V conversion and 81.7% for a 24 V-to-5 V conversion. With reconfigurable Gaussian regulations, EMI is reduced by increasing Gaussian switching rise/fall times from 3 ns to 7 ns at the expense of about 1.5% efficiency. With SSFD scheme, the efficiency reduction is less than 0.1% with 5% modulation range ($\frac{\Delta f_m}{f_0}$).

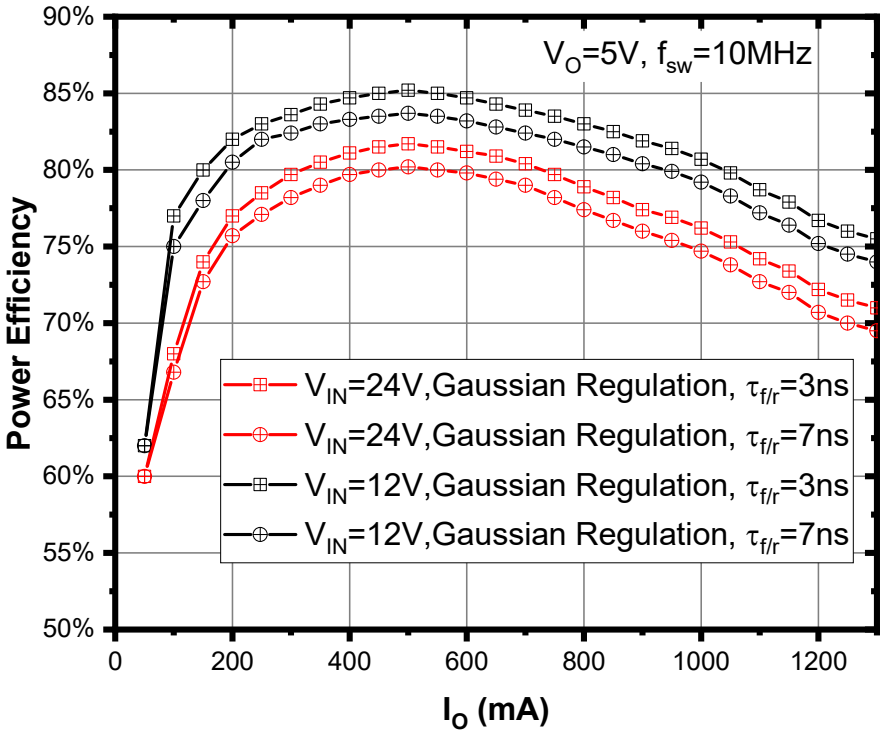


Figure 5.24: Measured power efficiency.

Table 5.1 shows the comparison of the presented Gaussian DC-DC converters with the prior arts. Compared to [38], it achieves 7x wider V_{IN} and 1.5x higher f_{SW}. By using the proposed Gaussian switching regulation, EMI noise is reduced by 49.1 dB at around 100 MHz which is 26.6 dB better than in [42] and is reduced by 36.9 dB at around 10 MHz which is 5.9 dB better than in [39]. The peak efficiency is 85.2% for 12 V-to-5 V conversion using Gaussian (τ_f=τ_r=3 ns) switching, comparable with trapezoidal switching [38, 39, 42, 43].

Based on the proposed three-level buck converter with Gaussian regulation and ZVS schemes, The simulated power efficiency of the proposed GaN-based three-level buck converter with Gaussian regulation and ZVS schemes is shown in Fig. 5.25. Compared to the two-level buck converter, the peak efficiency is 90.2% for 12 V-to-5 V conversion using Gaussian regulation and ZVS combined. Thanks to the three-level topology and ZVS schemes, the power efficiency is increased by 5%.

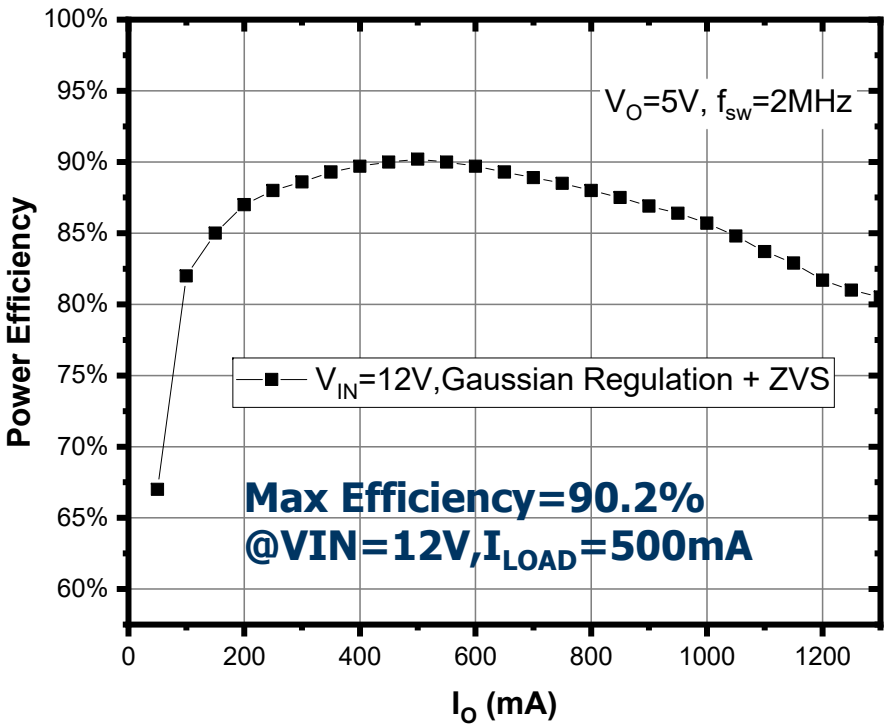


Figure 5.25: Simulated power efficiency of the proposed three-level buck converter with ZVS.

Chapter 6

Conclusion and Future Work

6.1 Magnetic-free Nonreciprocal Components

Two key magnetic-free nonreciprocal components, isolators and circulators, are demonstrated in 65nm CMOS process with isolation beyond 45 dB and the minimum insertion losses of 5.6 dB across 85-100 GHz. Utilizing resonant-type structures and feasible low-side modulation schemes, the isolator and circulator achieve spatio-temporal modulated nonreciprocity at 100 GHz band.

To increase the bandwidth of the proposed nonreciprocal components in the future, one possible solution is to use multiple nonreciprocal branches that operate concurrently with shared passive components to control the chip area [57]. Another approach is to replace the mixing stages by the wideband ones such as Gilbert units as in [22].

With the reconfigurable high isolation, the isolator can separate different RF channels with high isolations or connect them with low insertion losses. The circulator can have the high TX-RX isolation in on-chip full-duplex transceiver. The proposed two designs can be used in full-duplex on-chip transceivers for ultra-high data rate wireless communication at mm-wave/sub-THz bands.

6.2 Gaussian Regulated Gate Driver

The first on-chip Gaussian switching regulation scheme is demonstrated in GaN gate driver to reduce the EMI noise in the high-frequency domain. Utilizing SSFD scheme, the EMI noise at low-frequency domain is effectively reduced without sacrificing power efficiency and the Gaussian switching Regulation also effectively reduces EMI noise in the high-frequency domain caused by the SSFD scheme alone. To handle the high switching frequency and reduce the system size and power, feed-forward control scheme is adopted to produce the Gaussian switching regulation in GaN switch without introducing feedback loop and Gaus-

sian reference into the driver. To optimize the power efficiency versus EMI noise level, the reconfigurable slope Gaussian switching regulation is utilized in the proposed work. Experimental results precisely agree with the theory and verify the effectiveness of the design techniques.

APPENDIX A

Publication list during Ph.D. program:

[58] C. Yang and P. Gui, "85-110-GHz CMOS Magnetic-Free Nonreciprocal Components for Full-Duplex Transceivers," in IEEE Journal of Solid-State Circuits, vol. 54, no. 2, pp. 368-379, Feb. 2019, doi: 10.1109/JSSC.2018.2875478.

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